

Model Name : Z5WAL
 File Name : LA-B211P

Compal Confidential

EA51_BM UMA M/B Schematics Document

Intel Bay Trail M

2014-04-07

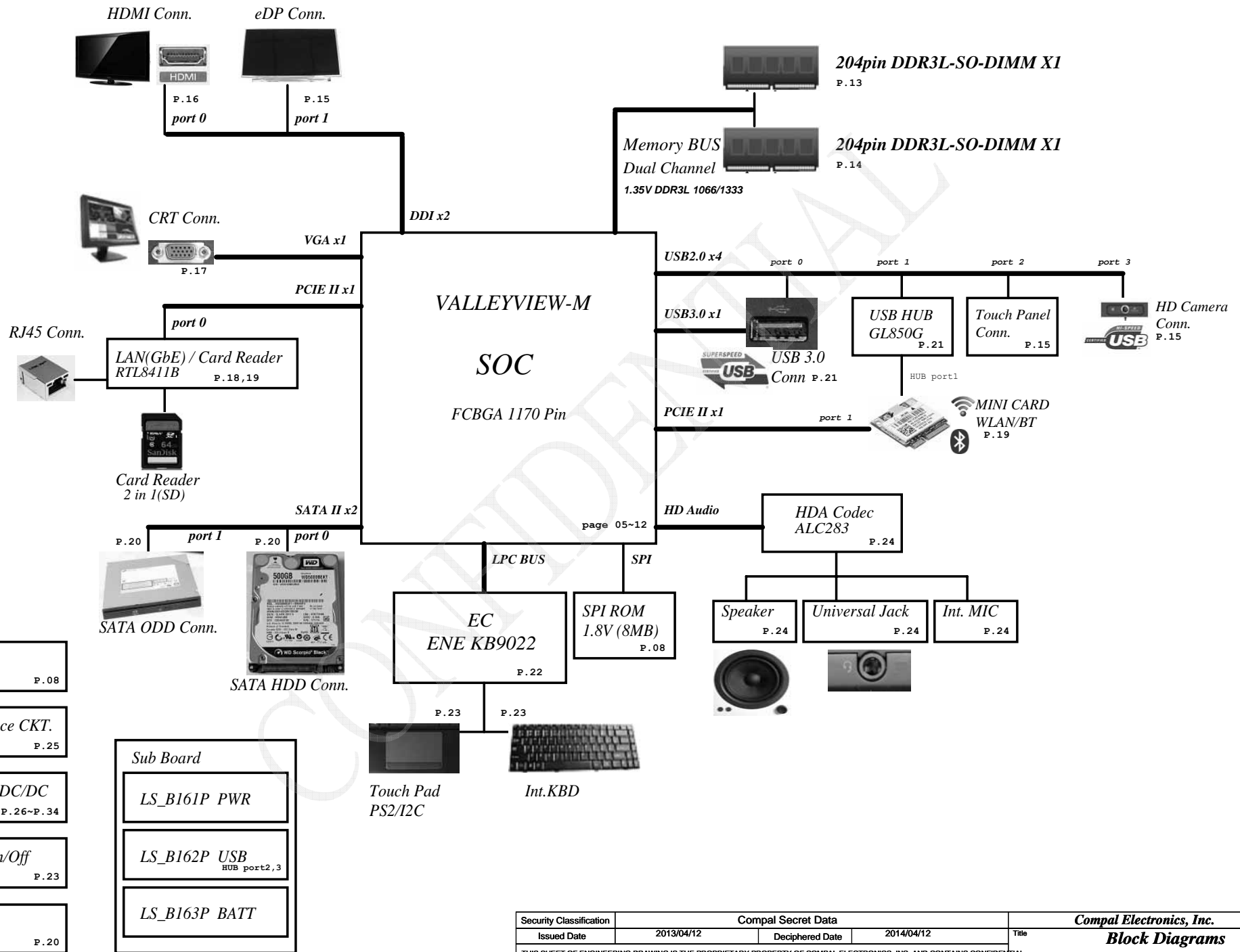
REV: 1.0

Panelization Information	
Main Board	LA-B211P
PWR Board	LS-B161P
USB Board	LS-B162P
BATT Board	LS-B163P

PCB@
 ZZZ PCB Z5WAL LA-B211P LS-B161P/B162P/B163P

Part Number	Description
DAZ15Y00100	PCB Z5WAL LA-B211P LS-B161P/B162P/B163P

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- RTC CKT. P. 08
- DC/DC Interface CKT. P. 25
- Power Circuit DC/DC P. 26~P. 34
- LED/Power On/Off P. 23
- Fan Control P. 20

- Sub Board
- LS_B161P PWR
 - LS_B162P USB HUB port2,3
 - LS_B163P BATT

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				Block Diagrams	
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Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.654 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

BOARD ID Table

Board ID	PCB Revision
0	
1	EVT
2	DVT
3	PVT
4	Pre-MP
5	
6	

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+3V_PTP	+3.3V power rail for PTP	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

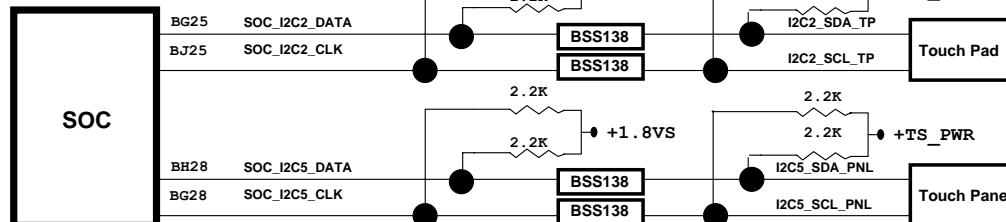
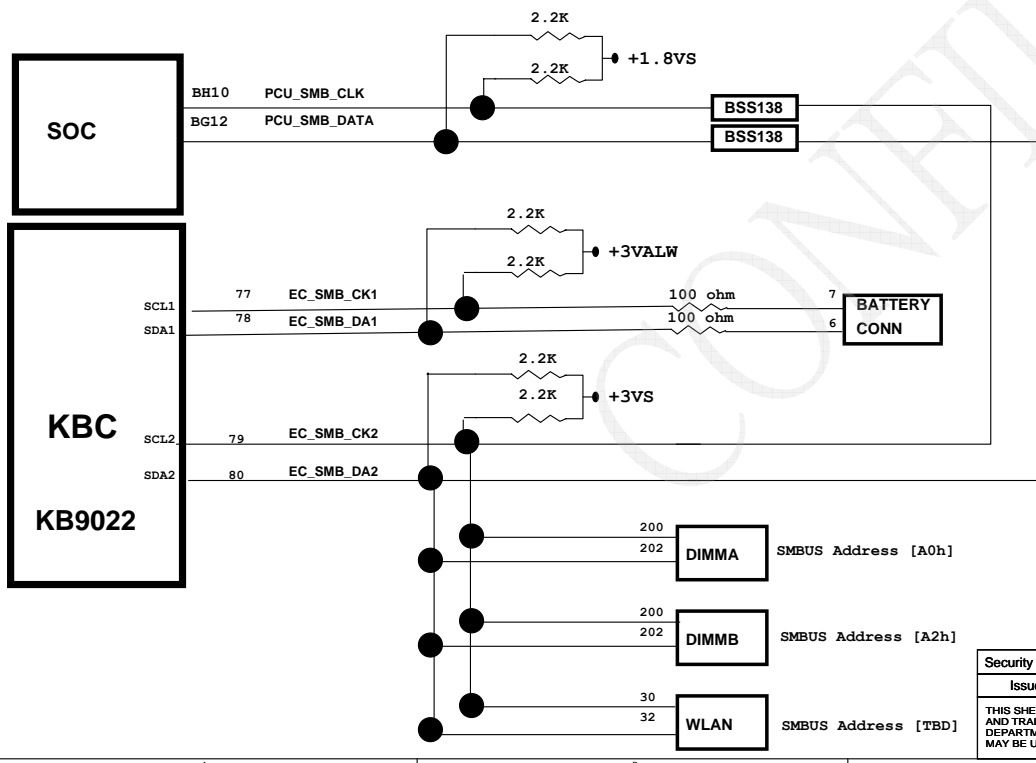
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

43 level BOM table

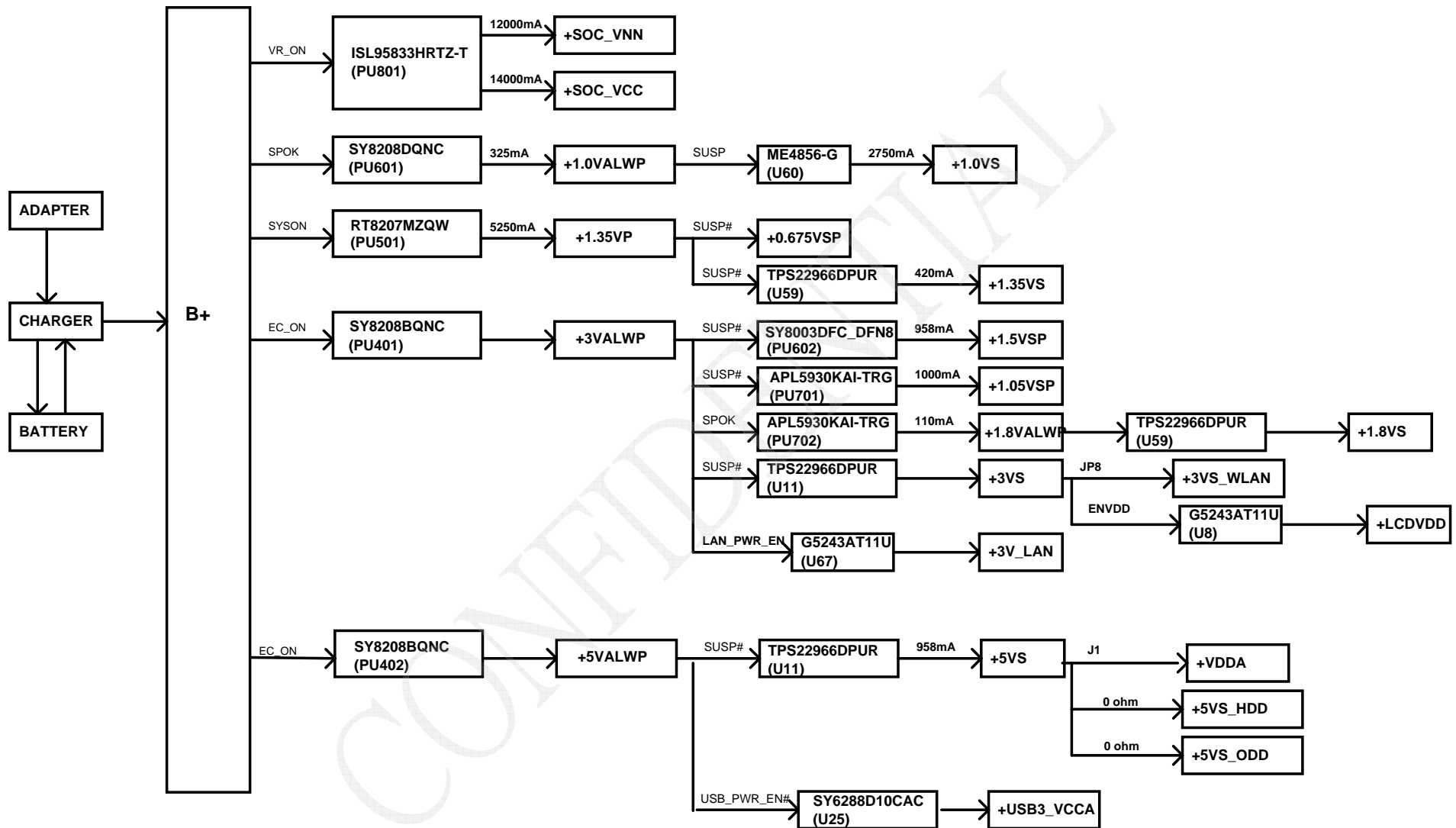
43 Level	Description	BOM Structure
4319SNBOL01	SMT MB AB211 25WAL UMA N2920 HDMI	N2920@/9022@/EMC@/PCB@/1DMIC@/NTPM@
4319SNBOL02	SMT MB AB211 25WAL UMA N3520 HDMI	N3520@/9022@/EMC@/PCB@/1DMIC@/NTPM@
4319SNBOL03	SMT MB AB211 25WAL UMA N3530 HDMI	N3530@/9022@/EMC@/PCB@/1DMIC@/NTPM@
4319SNBOL04	SMT MB AB211 25WAL UMA N2930 HDMI	N2930@/9022@/EMC@/PCB@/1DMIC@/NTPM@
4319SNBOL05	SMT MB AB211 25WAL UMA N2820 HDMI	N2820@/9022@/EMC@/PCB@/1DMIC@/NTPM@
4319SNBOL06	SMT MB AB211 25WAL UMA N2830 HDMI	N2830@/9022@/EMC@/PCB@/1DMIC@/NTPM@

BOM Option Table

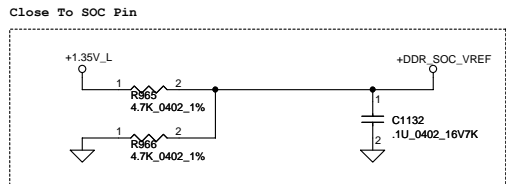
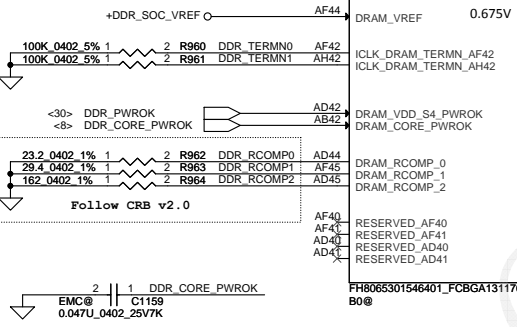
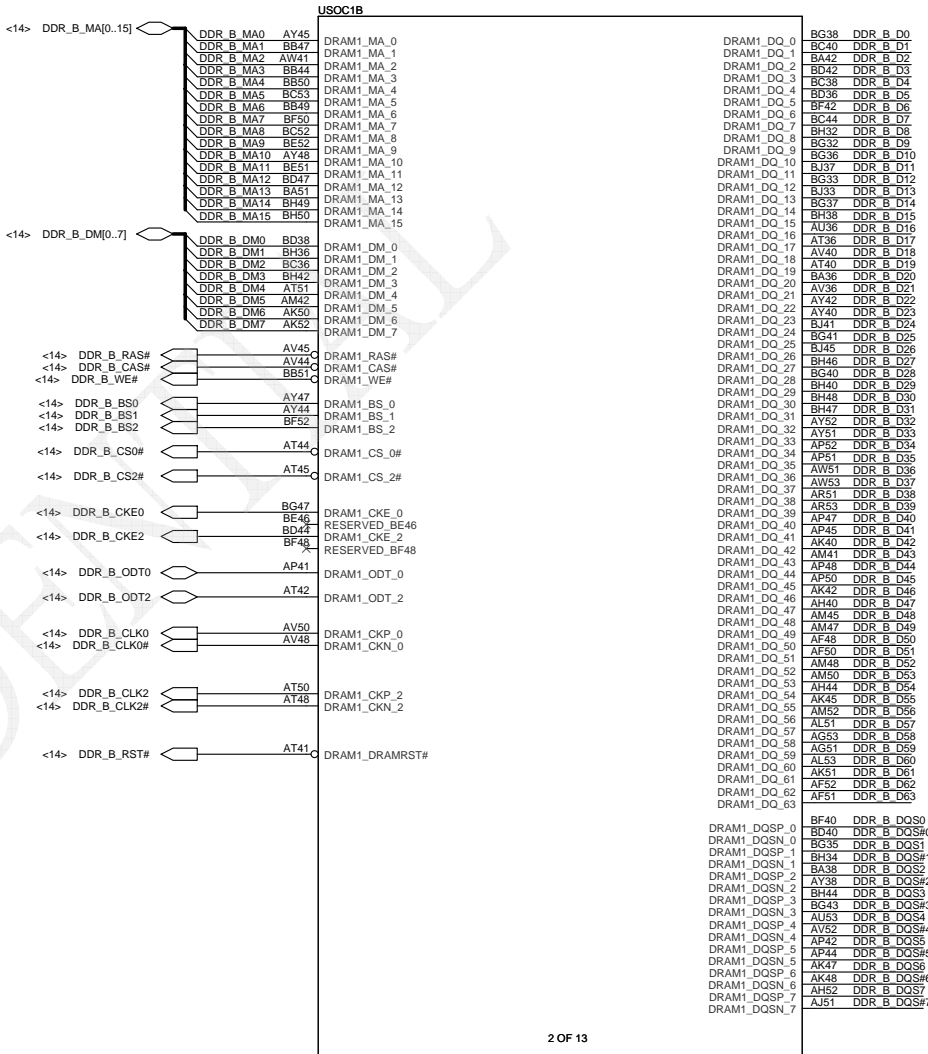
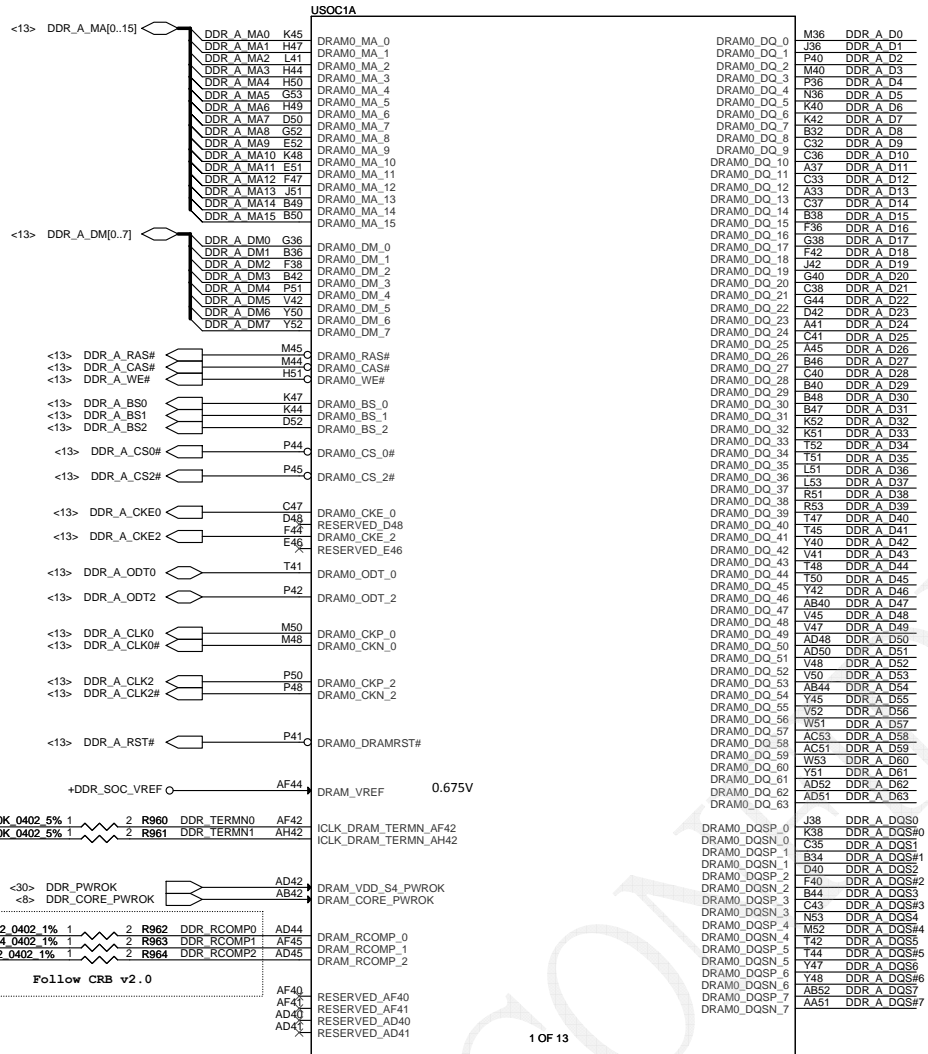
Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
KB9012	9012@
KB9022	9022@
Touch Screen I2C	TSI@
KB BL	BL@
DMIC*1	1DMIC@
DMIC*2	2DMIC@
TPM	TPM@
NTPM	NTPM@
Debug SW	DBG@



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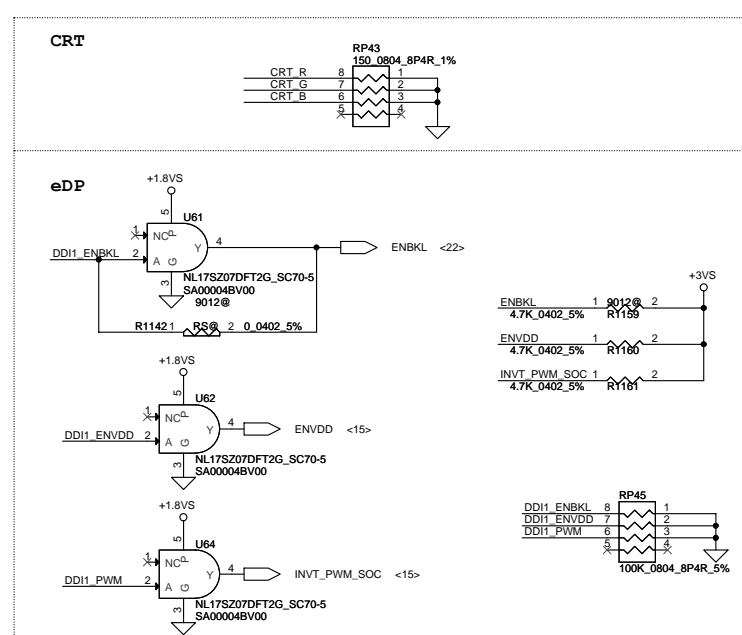
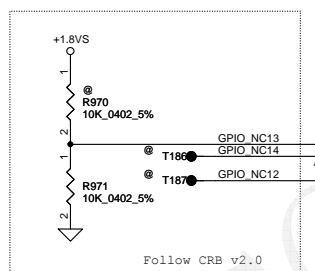
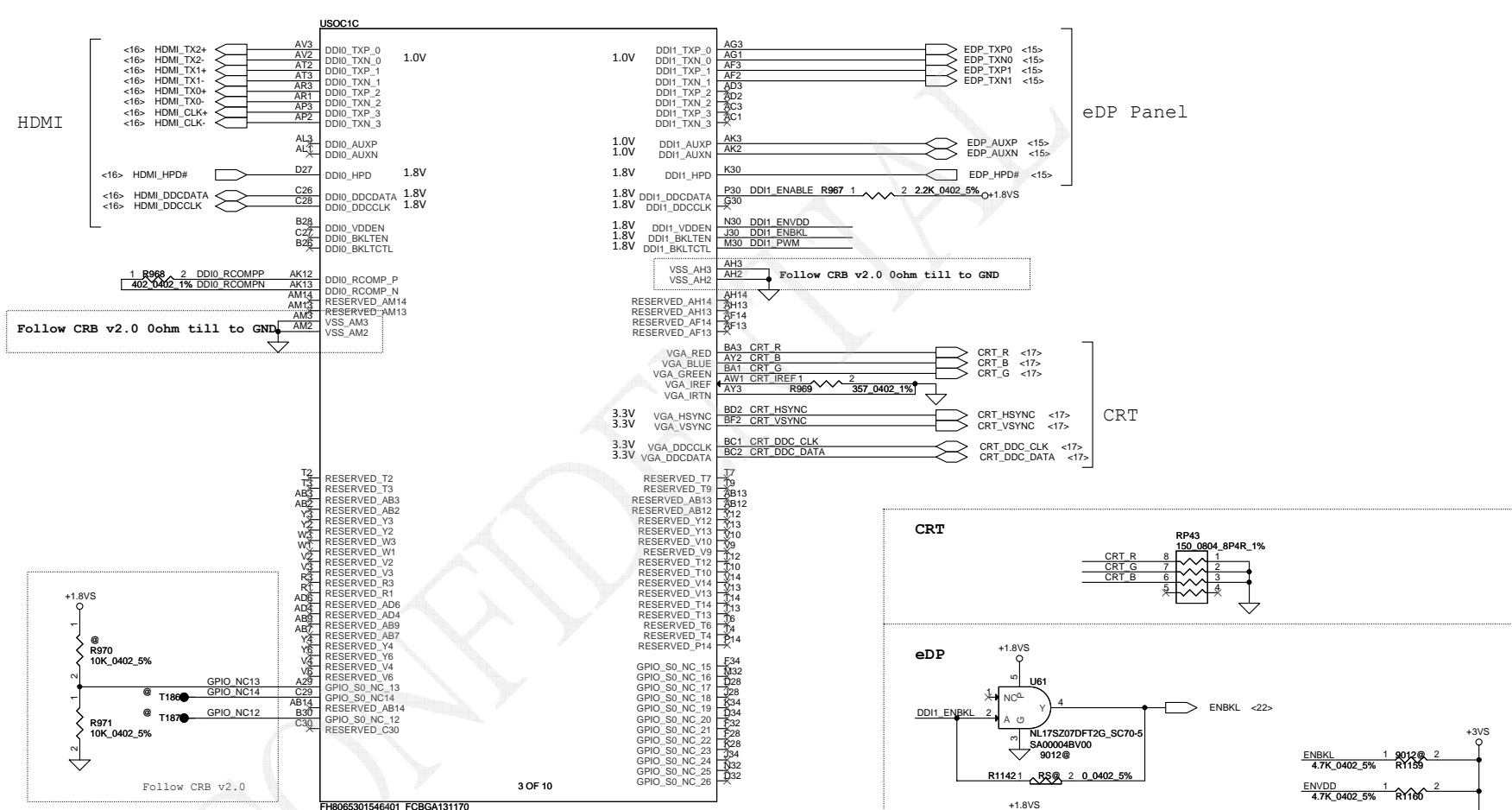


USOC1 N2830@
USOC1 N2930@
USOC1 N3530@

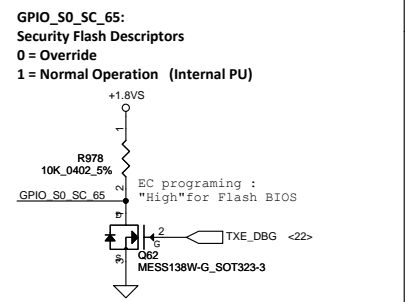
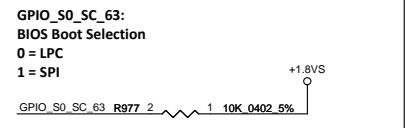
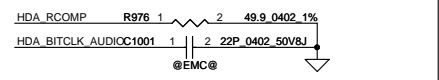
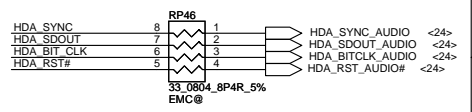
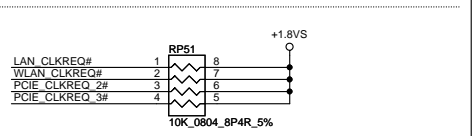
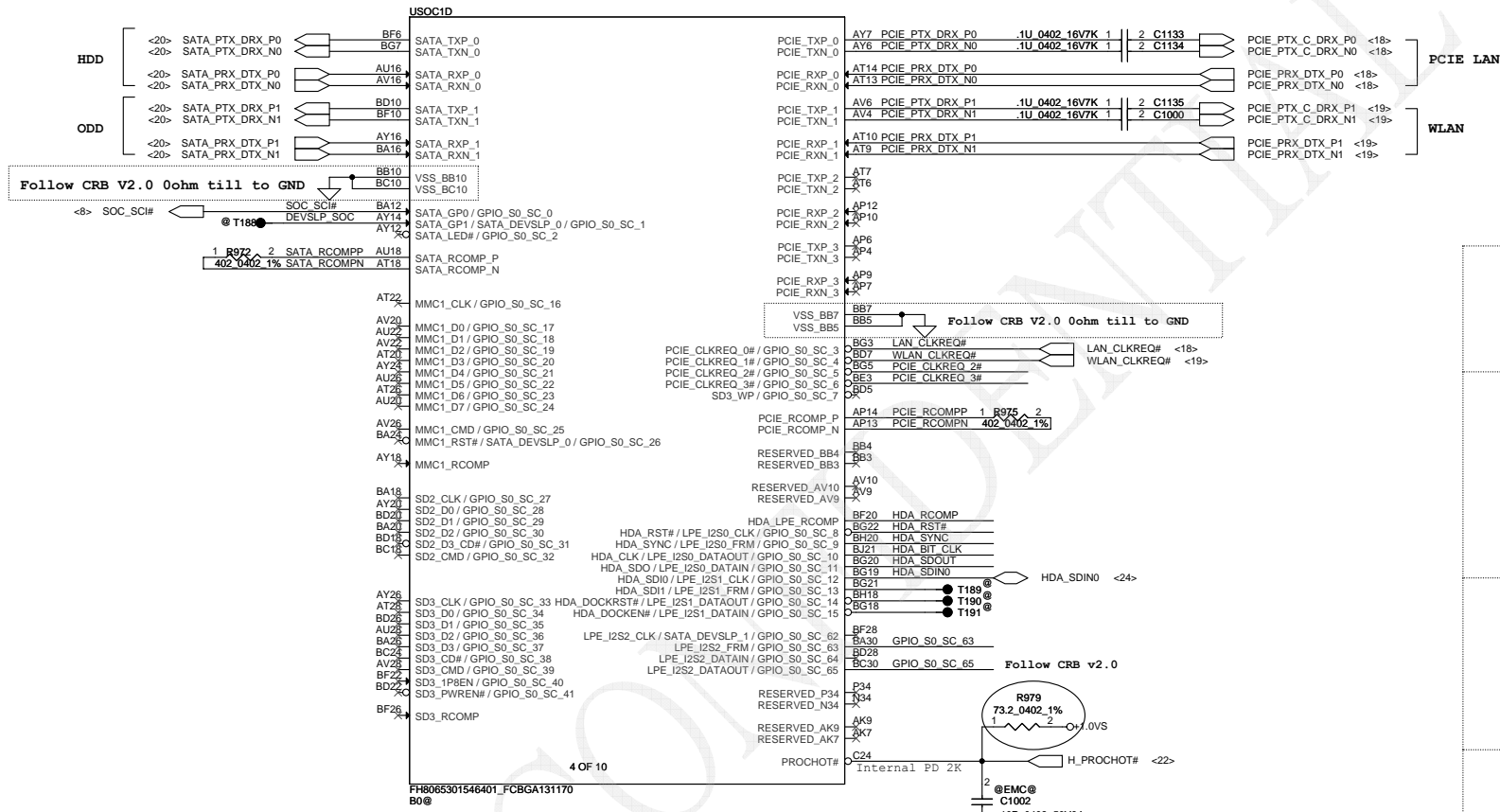
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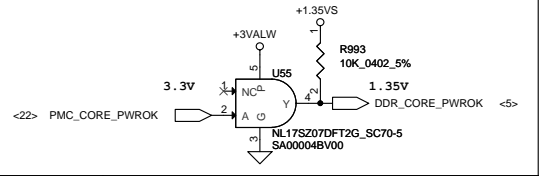
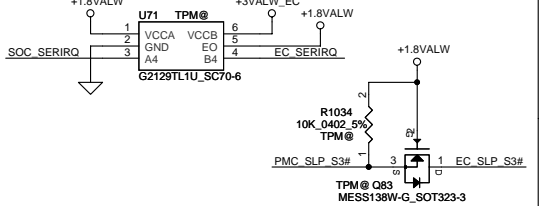
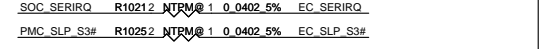
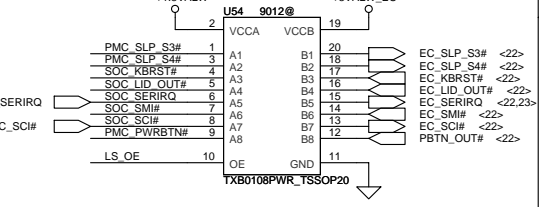
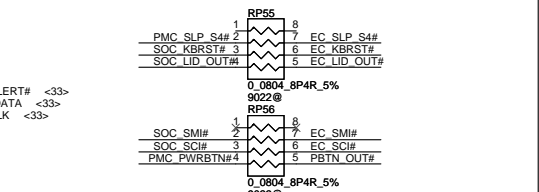
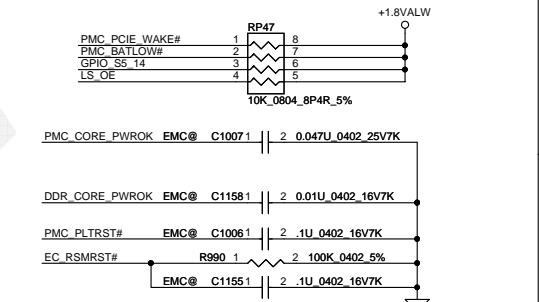
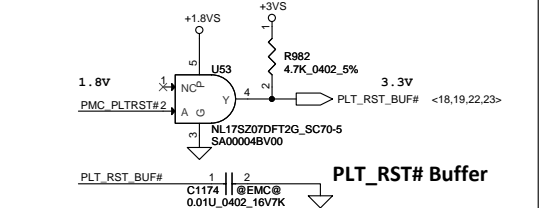
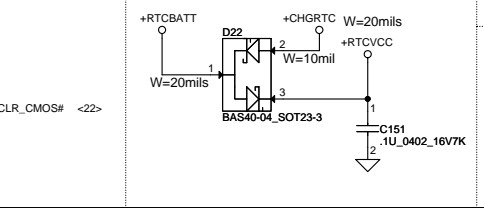
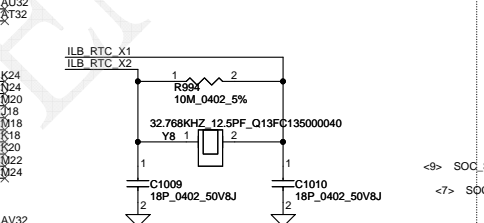
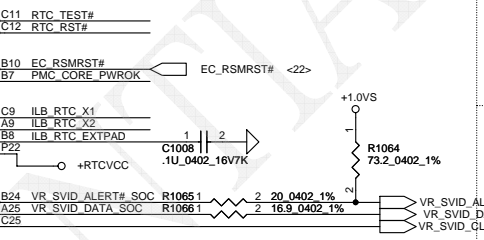
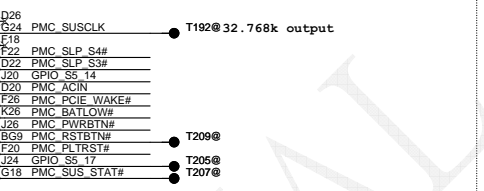
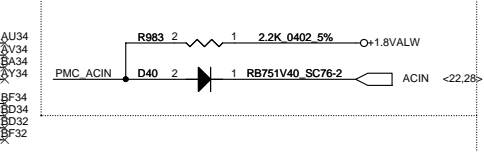
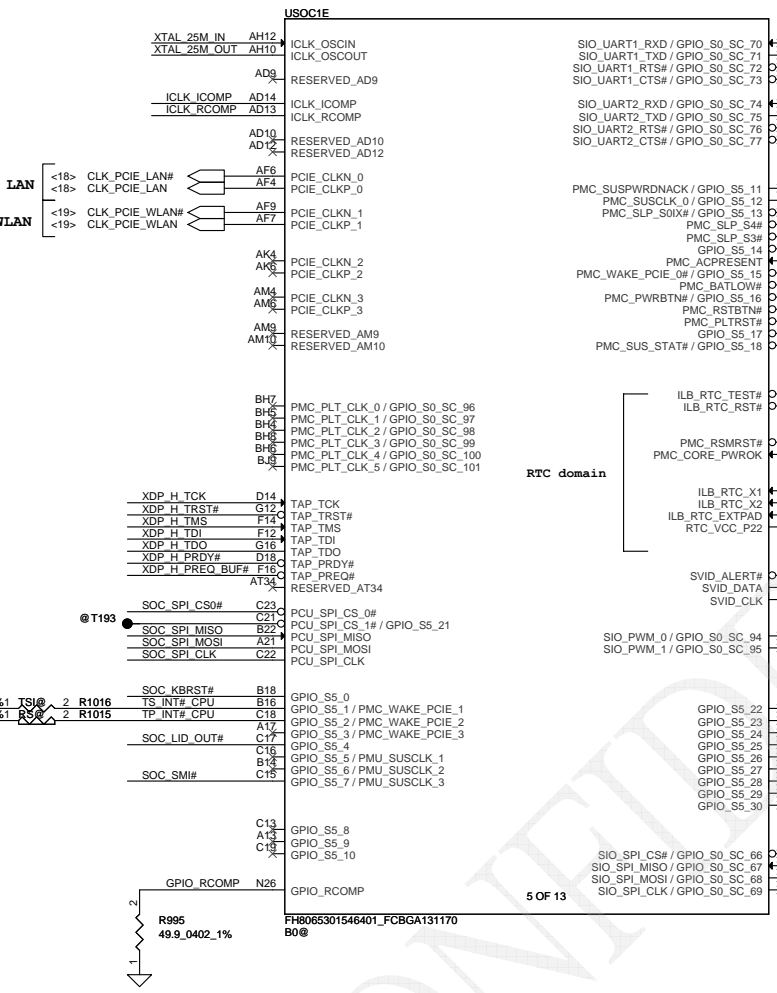
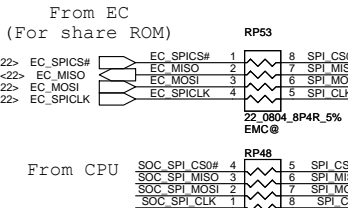
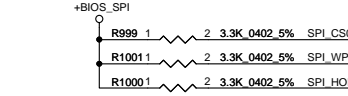
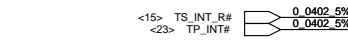
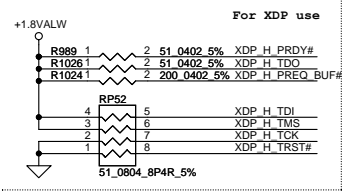
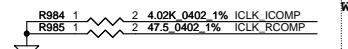
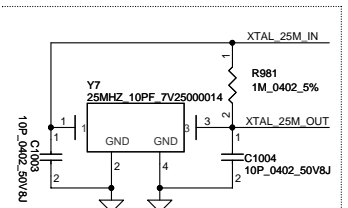
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VLV-M SOC Memory DDR3L	
Title	VLV-M SOC Memory DDR3L
Document Number	Z5WAL Bay Trail M LA-B211P
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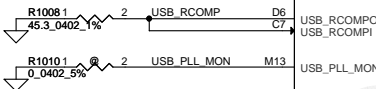
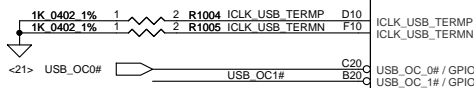
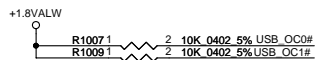
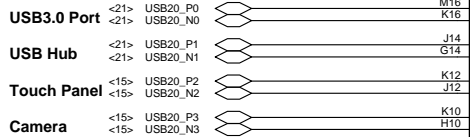
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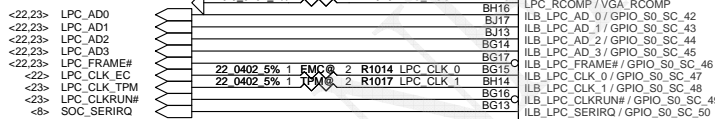
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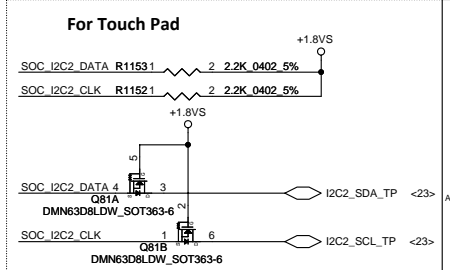
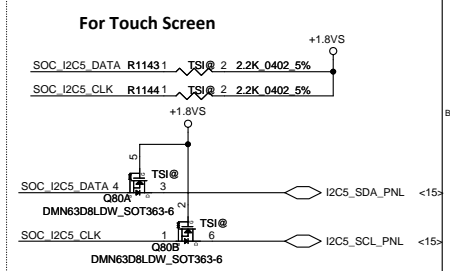
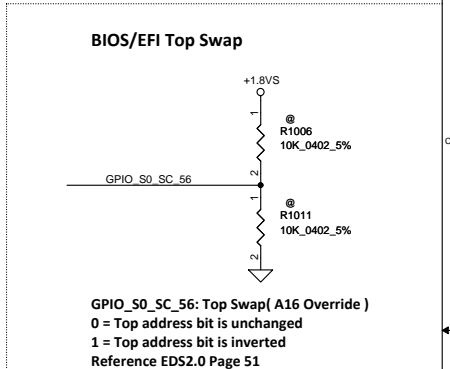
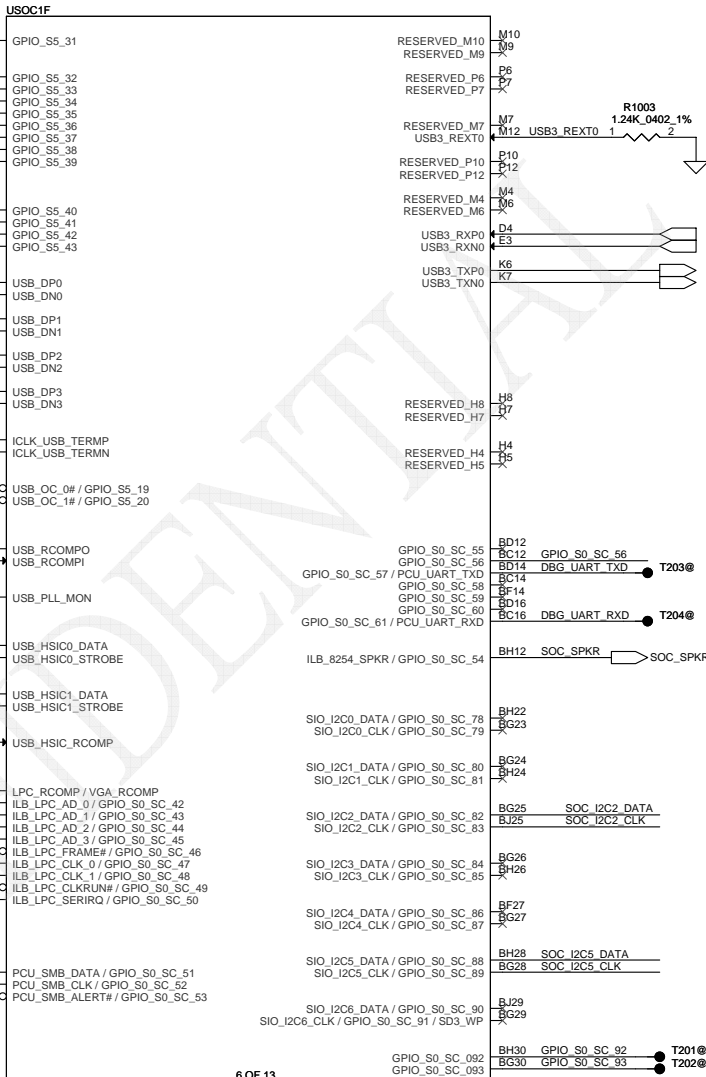


NOTE: Ref checklist rev1.2 p.25
USB_HSIC_RCOMP must NOT float if they are not being used.



**ILB_LPC_CLK_0 : Output of 25MHz,
Need Check with EC**

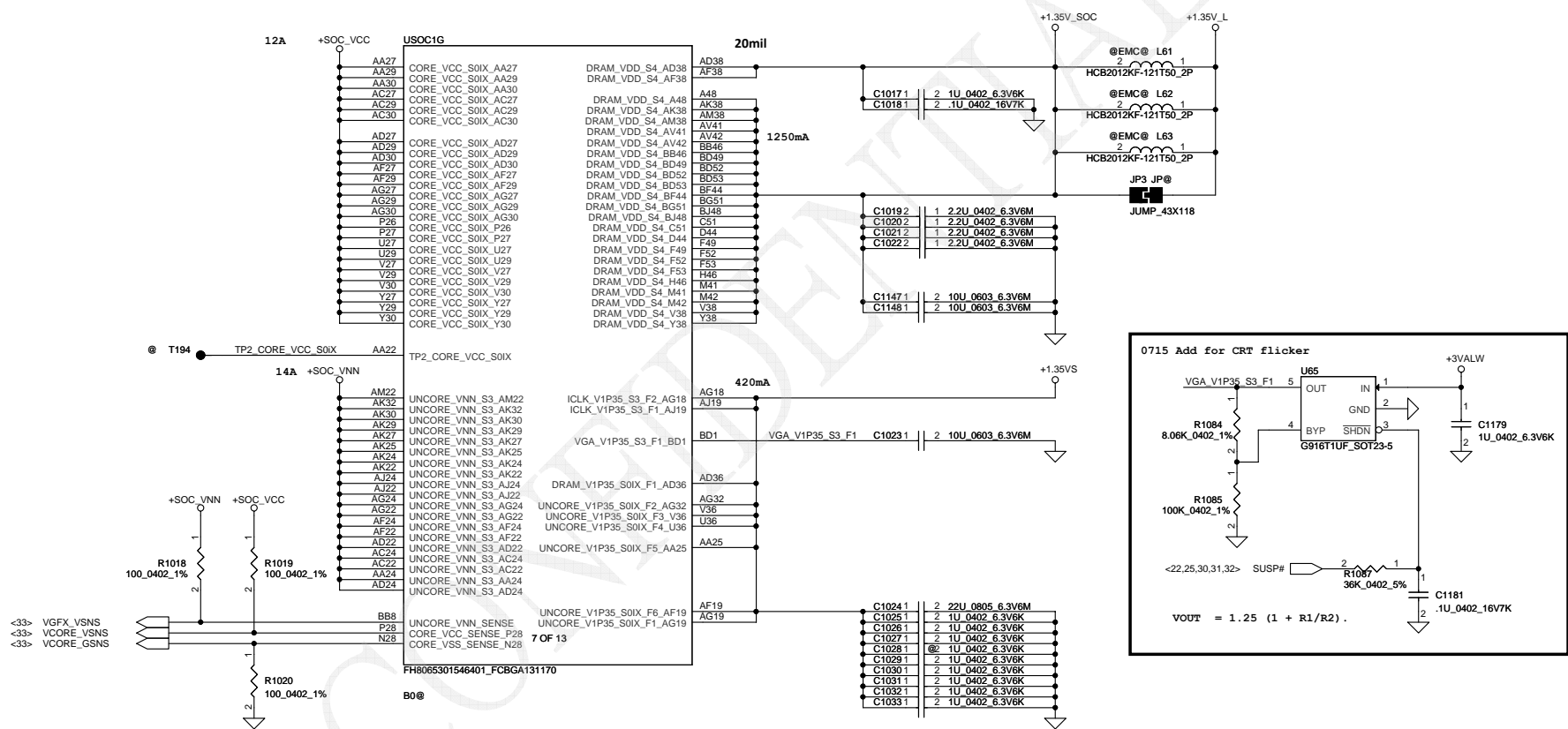
**ILB_LPC_CLK_1 is for CLK_0 feedback.(Input)
Set to Output for Normal Usage**



6 OF 13
FH8065301546401_FCBGA131170
B0@

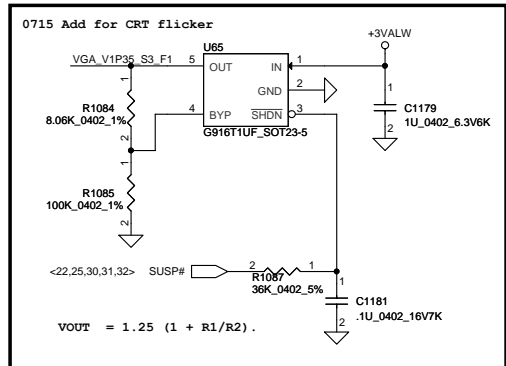
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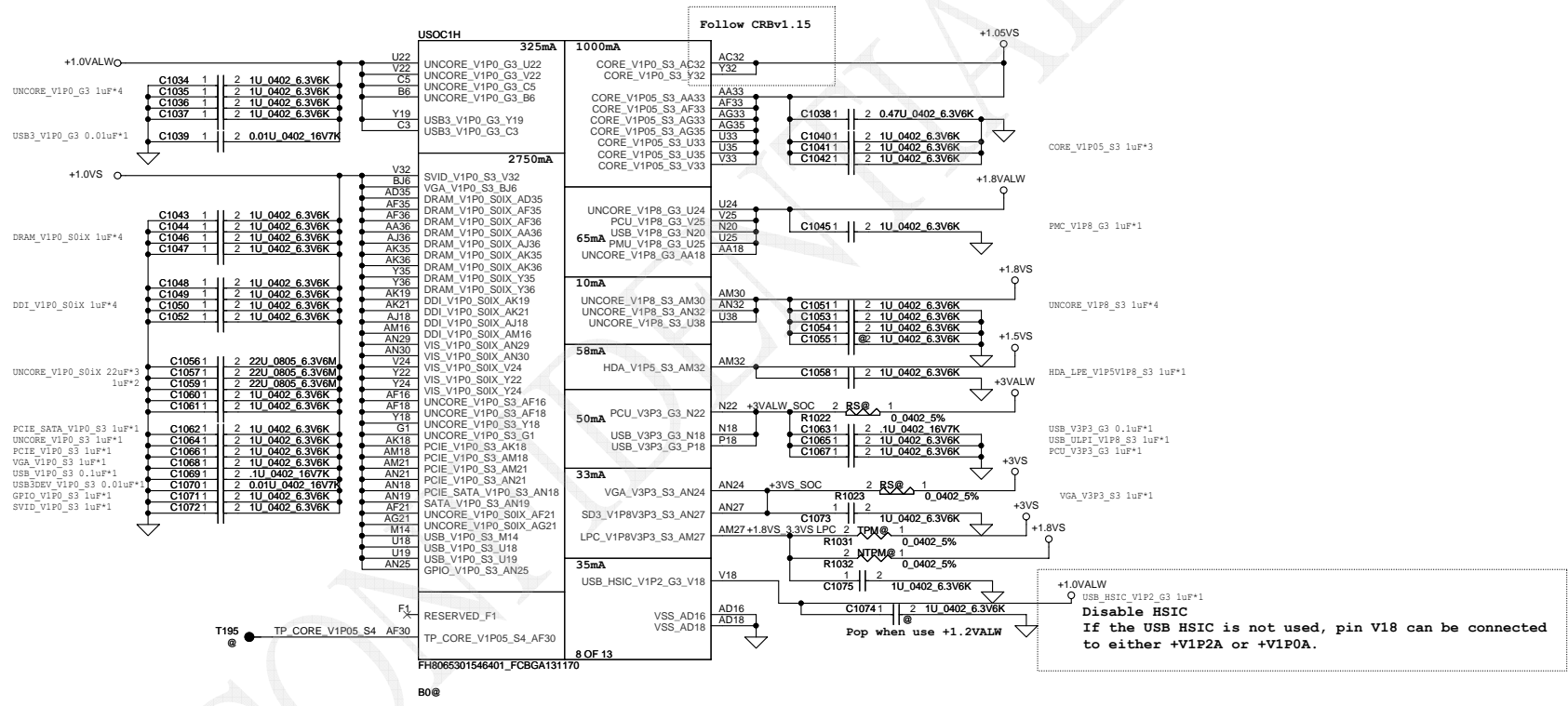


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 <33> VCORE_VSNS
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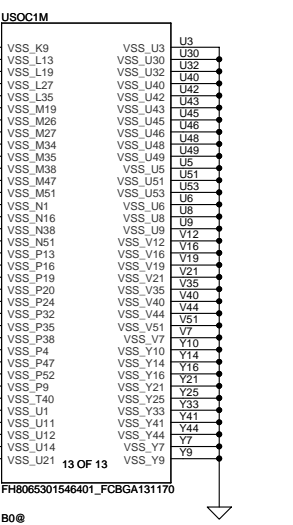
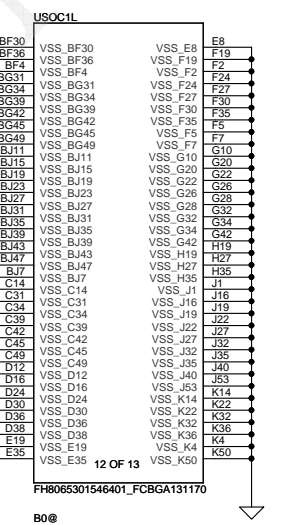
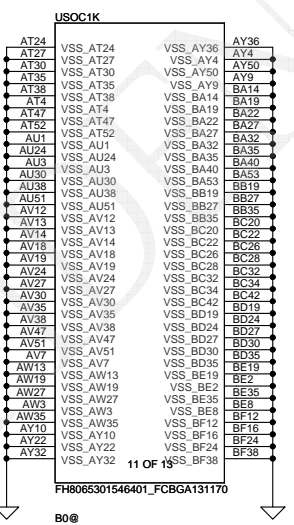
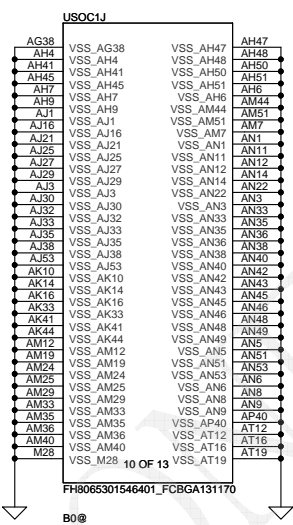
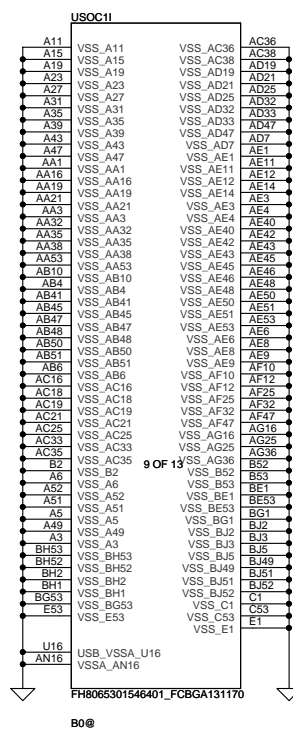
7 OF 13



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				Custom	1.0
				ZSWAL Bay Trail M LA-B211P	
				Date: Monday, April 07, 2014	Sheet 11 of 39

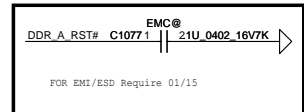
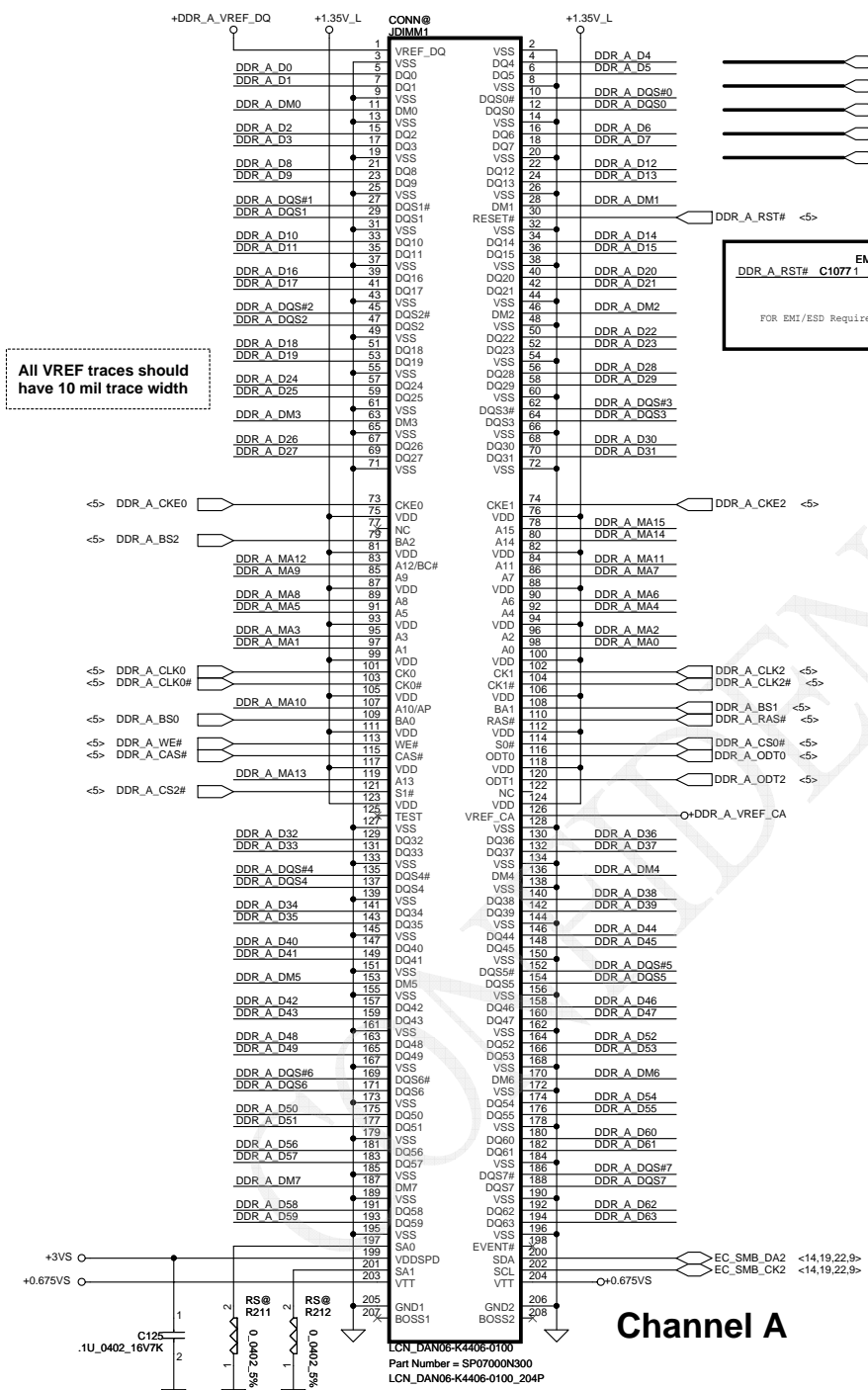


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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Rev 1.0
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Date: Monday, April 07, 2014				Sheet 12 of 39

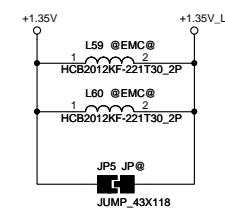
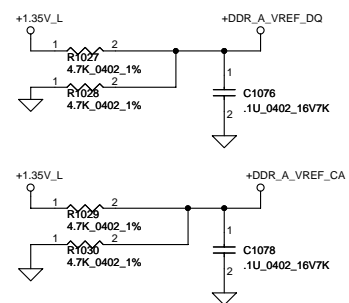
Compal Electronics, Inc.

VLV-M SOC GND

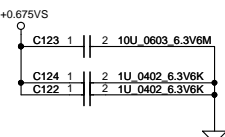
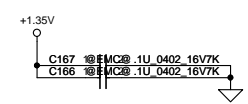
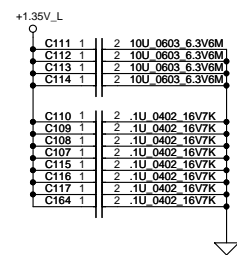
Customer: Z5WAL Bay Trail M LA-B211P



Signal voltage level = 0.675 V
 PLACE TWO 4.7K RESISTORS CLOSE TO DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
 Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.



Layout Note:
Place near JDIMM1



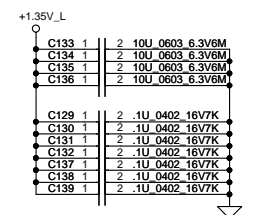
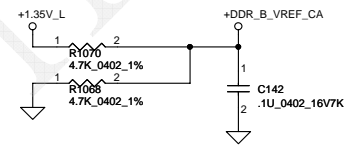
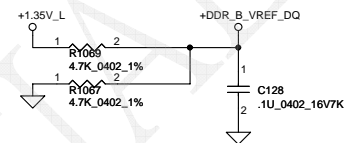
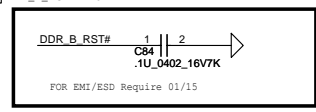
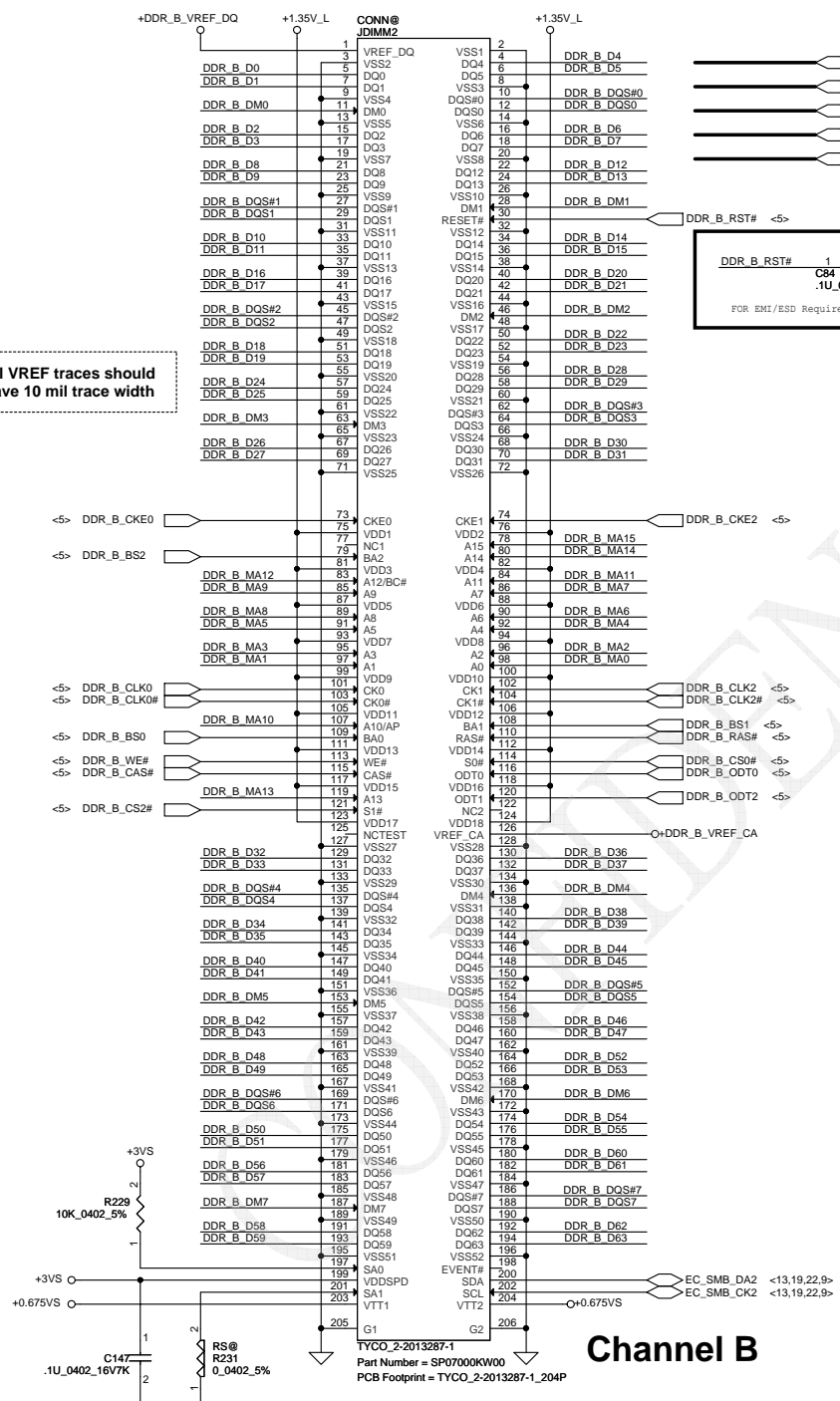
Layout Note:
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Channel A

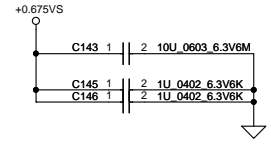
<Address: SA1:SA0=00 (A0H)>
DIMM_1 STD H:4mm

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All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204

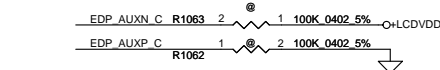
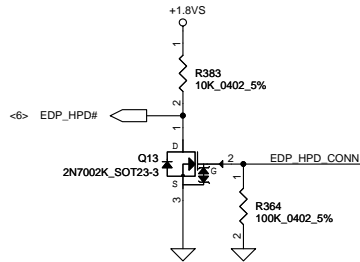
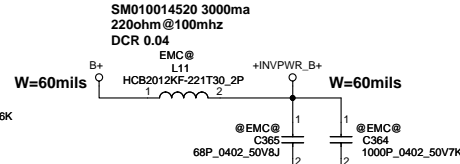
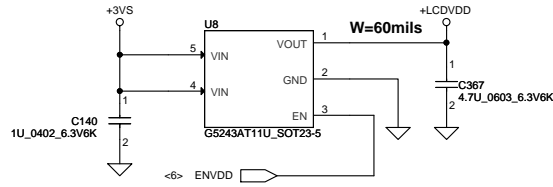
Channel B

TYCO_2-2013287-1
Part Number = SP07000KW00
PCB Footprint = TYCO_2-2013287-1_204P

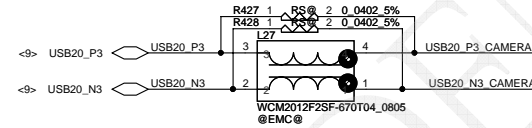
SA0/SA1 Follow INTEL demo board
<Address: SA0:SA1=10 (A2H)>
DIMM_2 REV H:4mm

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Customer	Document Number	Rev		Date	
	ZSWAL Bay Trail M LA-B211P	1.0		Monday, April 07, 2014	
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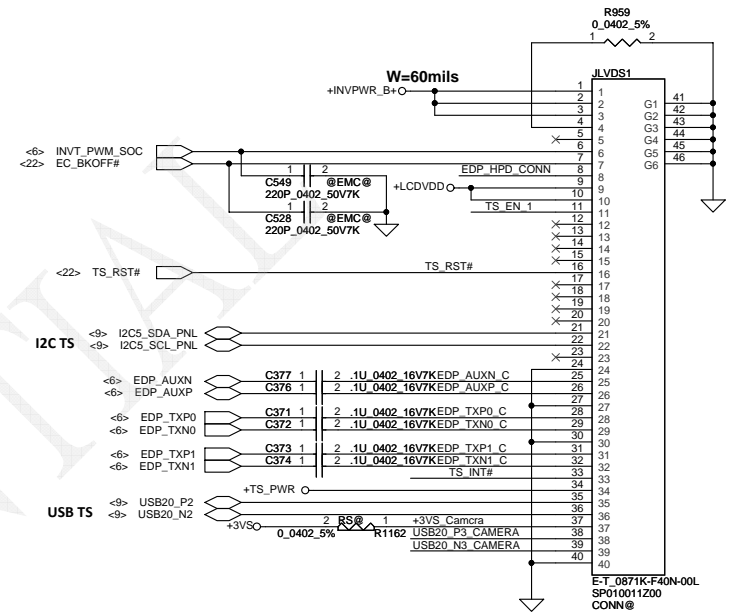
LCD POWER CIRCUIT



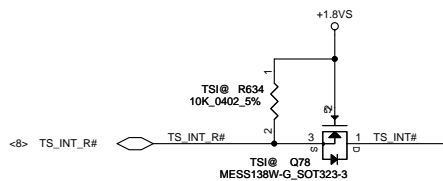
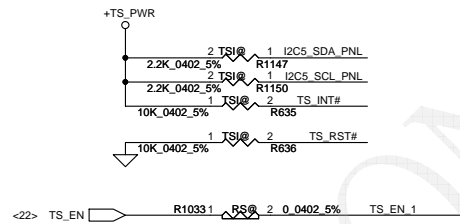
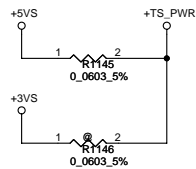
Intel recommends having a pull-up resistor of 100 kΩ for AUXN and a pull-down resistor of 100 kΩ for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.



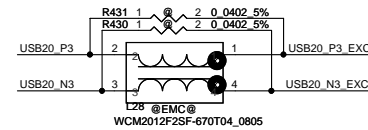
LCD/ LED PANEL Conn.



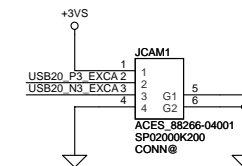
For Touch Panel



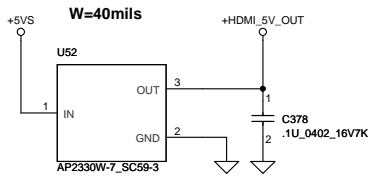
Camera reserve



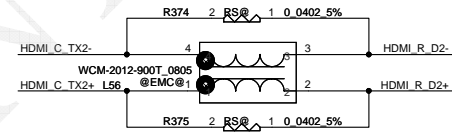
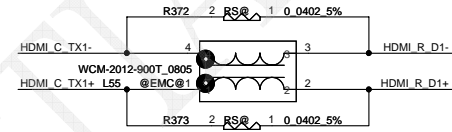
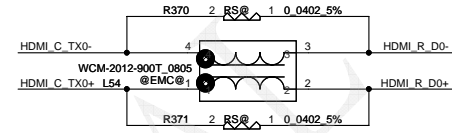
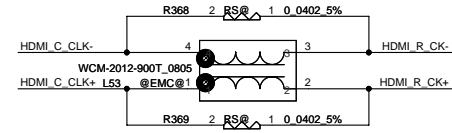
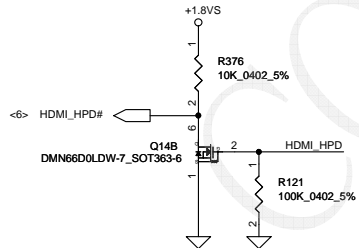
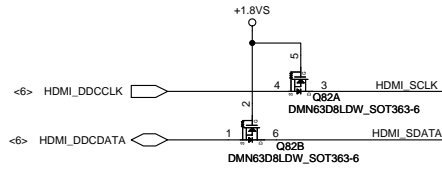
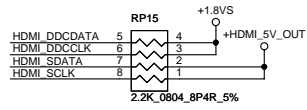
pin define, need to confirm



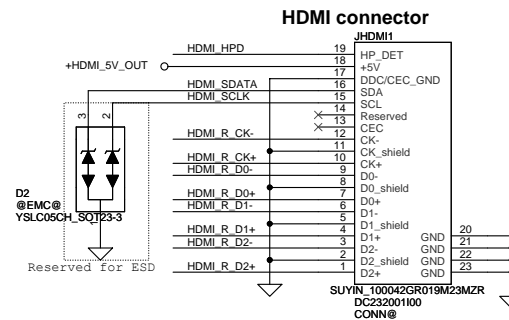
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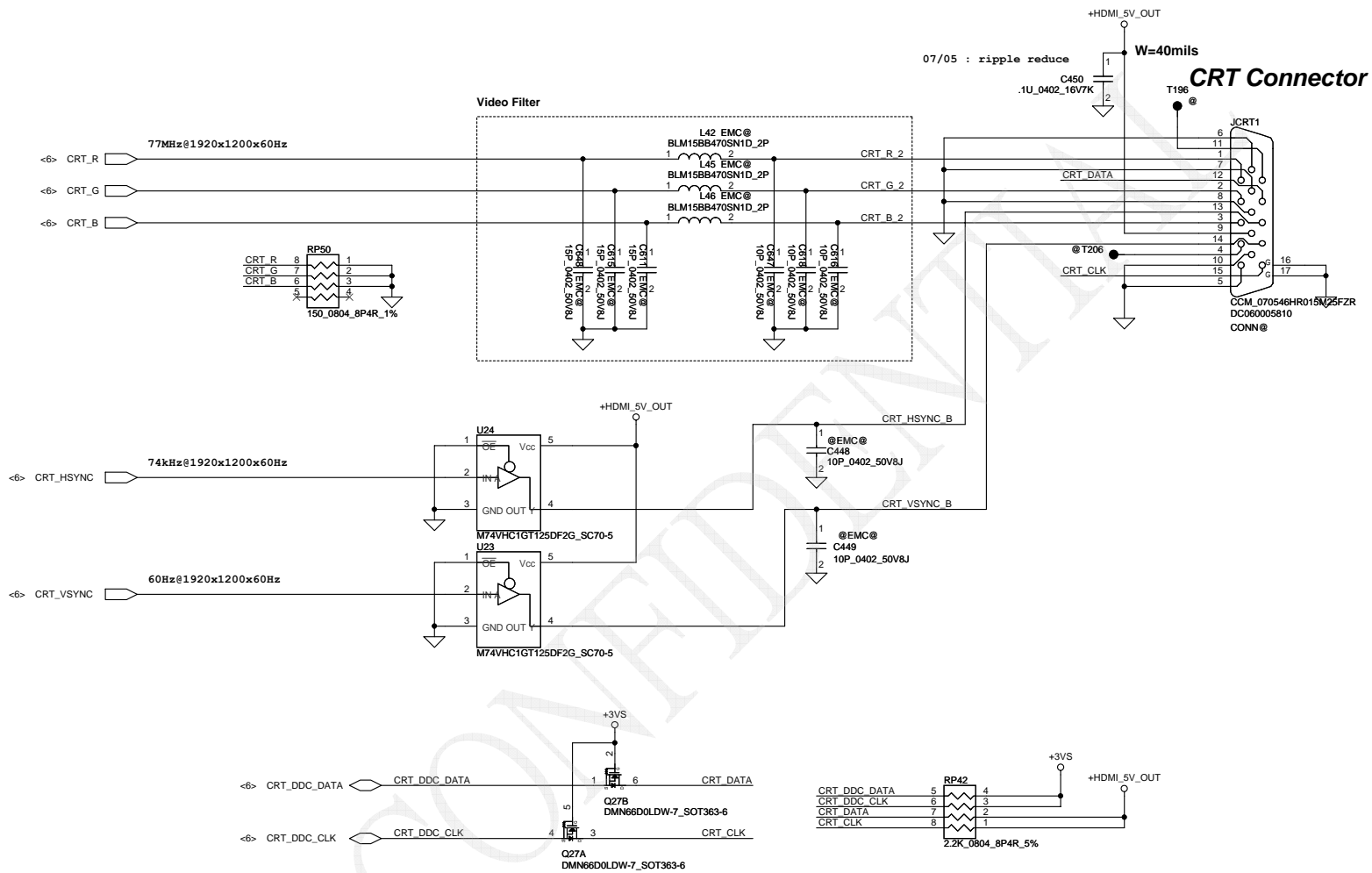
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<6>	HDMI_TX2-	C379	2	1	.1U_0402_16V7K	HDMI_C_TX2-
<6>	HDMI_TX2+	C380	2	1	.1U_0402_16V7K	HDMI_C_TX2+
<6>	HDMI_TX0-	C383	2	1	.1U_0402_16V7K	HDMI_C_TX0-
<6>	HDMI_TX0+	C384	2	1	.1U_0402_16V7K	HDMI_C_TX0+
<6>	HDMI_CLK-	C385	2	1	.1U_0402_16V7K	HDMI_C_CLK-
<6>	HDMI_CLK+	C386	2	1	.1U_0402_16V7K	HDMI_C_CLK+



HDMI_C_TX1-	R1071	1	2	619_0402_1%
HDMI_C_TX1+	R1072	1	2	619_0402_1%
HDMI_C_TX2-	R1073	1	2	619_0402_1%
HDMI_C_TX2+	R1074	1	2	619_0402_1%
HDMI_C_TX0-	R1075	1	2	619_0402_1%
HDMI_C_TX0+	R1076	1	2	619_0402_1%
HDMI_C_CLK-	R1077	1	2	619_0402_1%
HDMI_C_CLK+	R1078	1	2	619_0402_1%



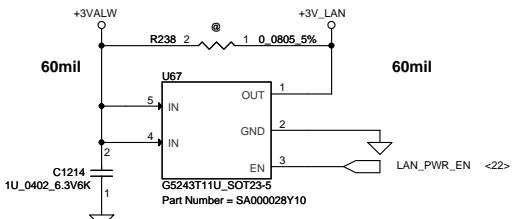
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CRT CONN.

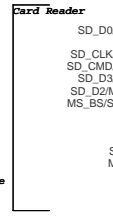
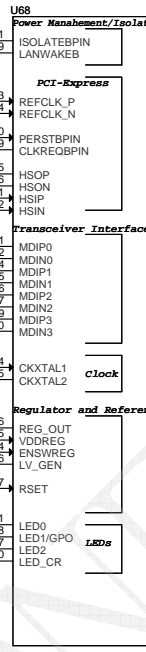
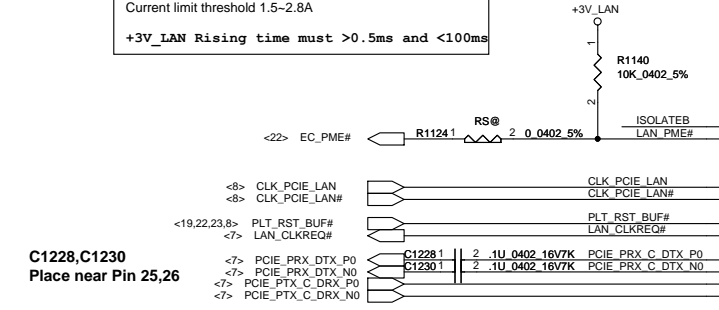
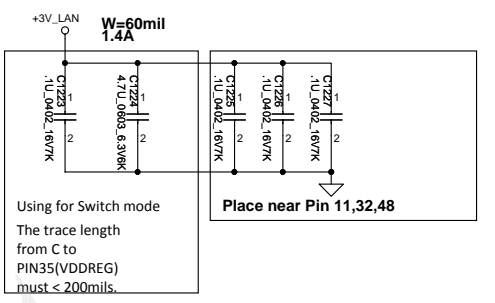
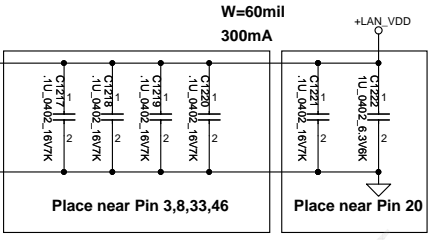
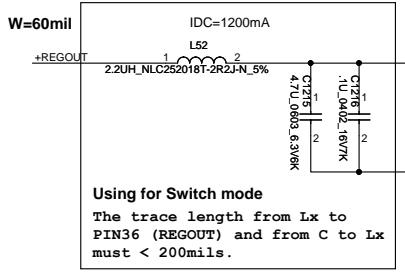
ZSWAL Bay Trail M LA-B211P



From EC

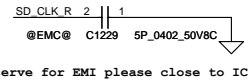
High active.
 EN threshold voltage min:1.2V typ:1.6V max:2.0V
 Current limit threshold 1.5-2.8A

+3V_LAN Rising time must >0.5ms and <100ms

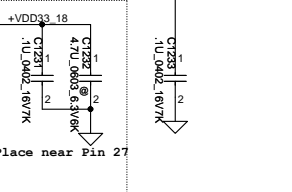
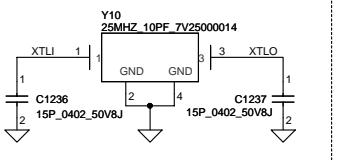
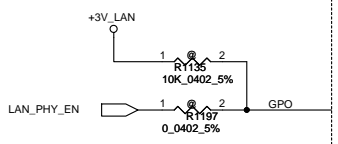
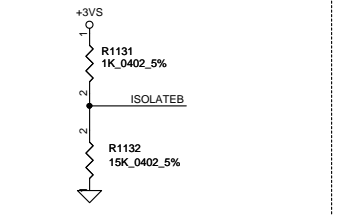


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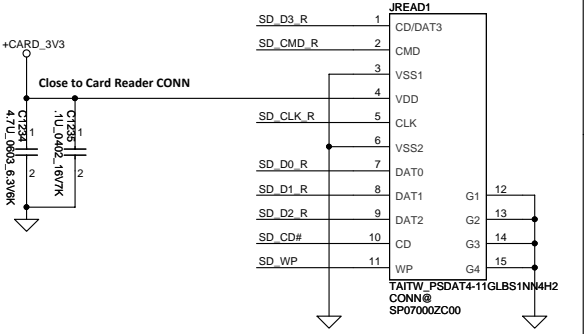
Internal pull high



	Write protect (Lock)	Write protect (Unlock)	Card Detect
Without Card	Open	Open	Open
Card Inserted	Open	Close	Close



Card Reader Connector

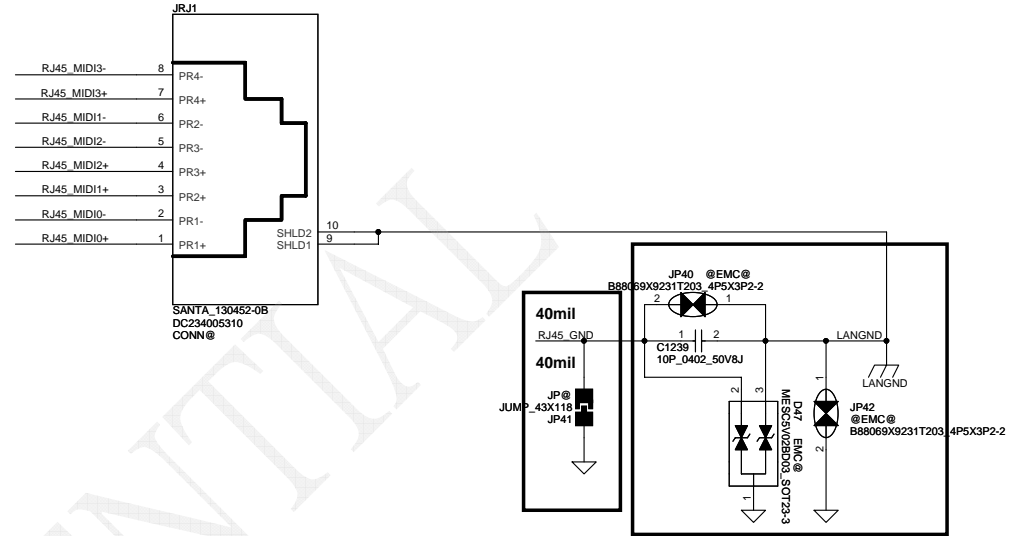
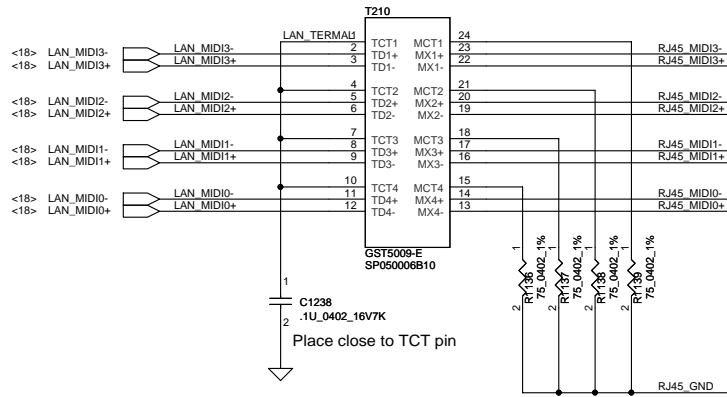


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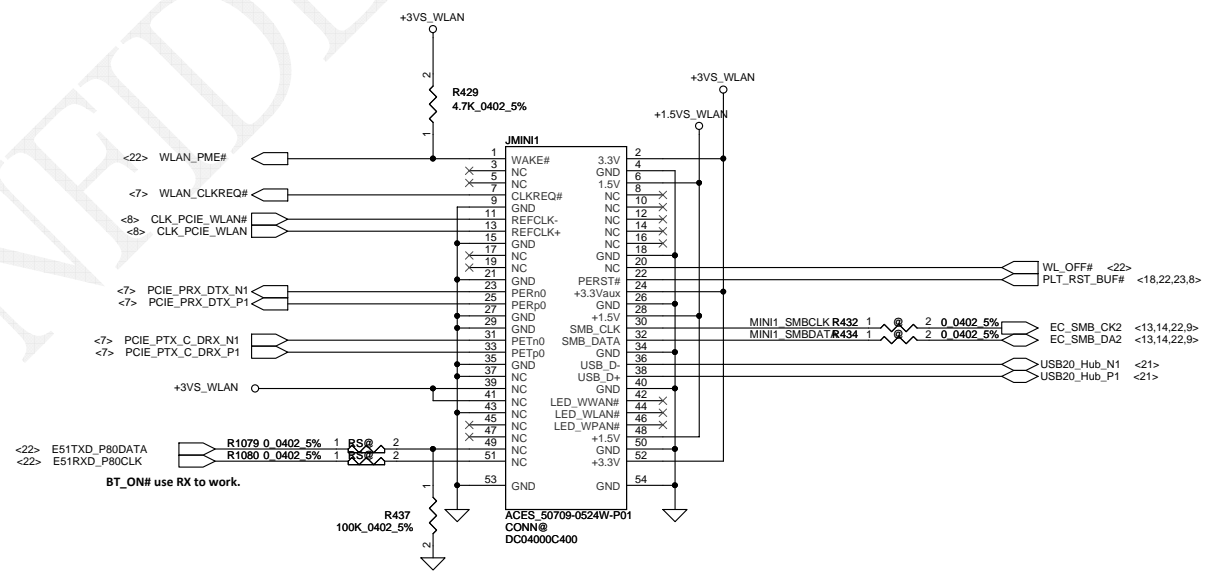
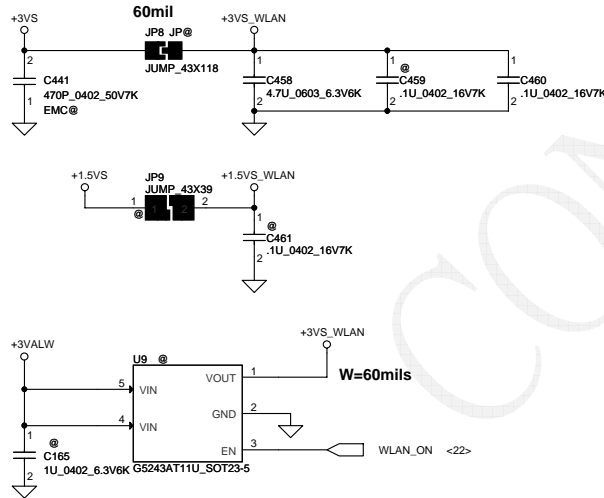
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Compal Electronics, Inc.	
LAN RTL8411B-CG	
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LAN Connector

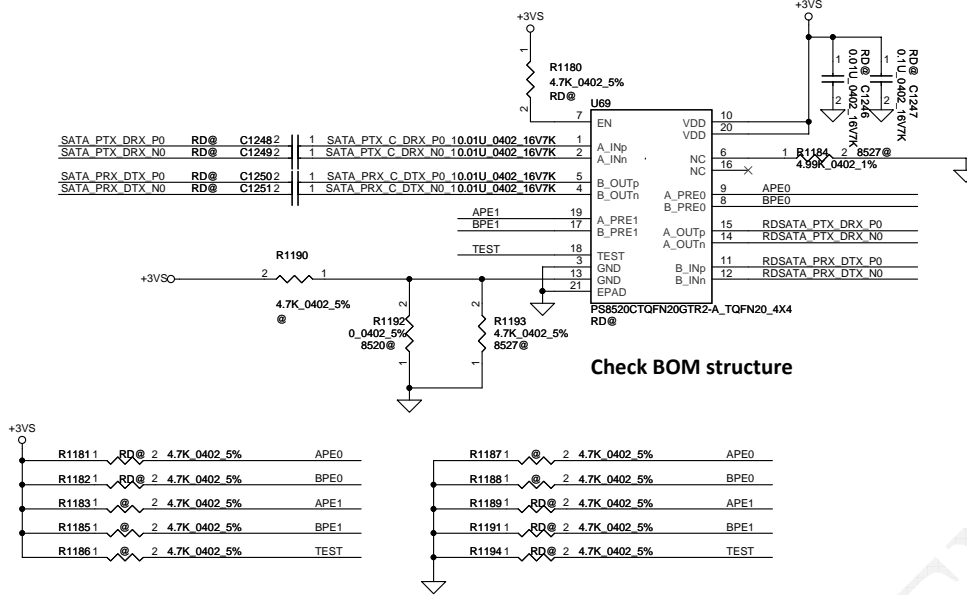


For Wireless LAN

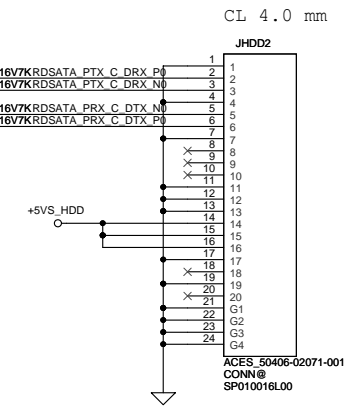


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				LAN/WLAN/BT
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Date: Monday, April 07, 2014				Sheet 19 of 39

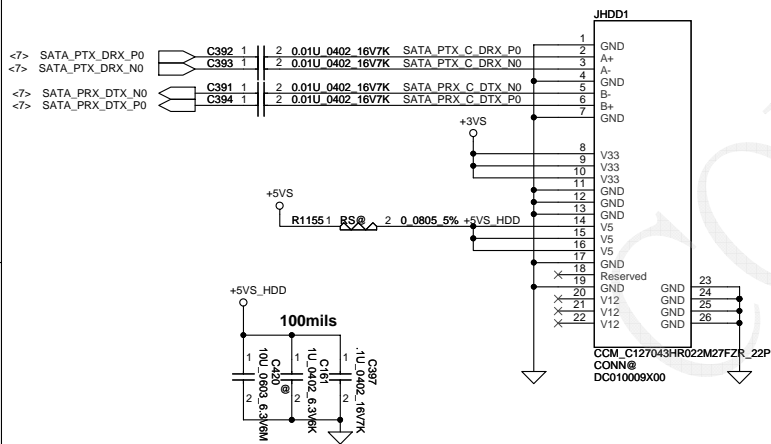
SATA Re-Driver HDD2 Conn. Reserve



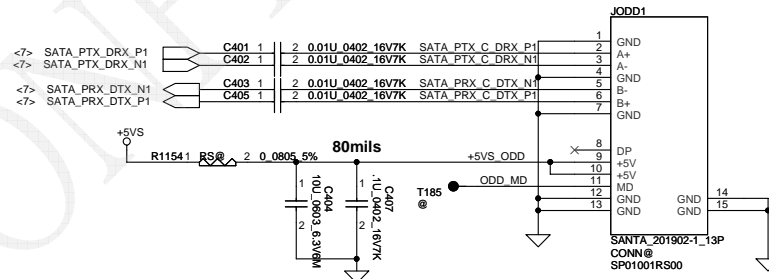
SATA HDD2 Cable Conn.



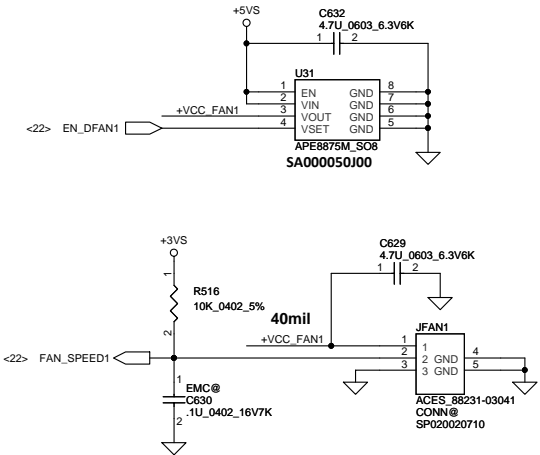
SATA HDD1 Conn.



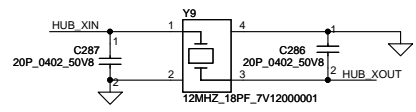
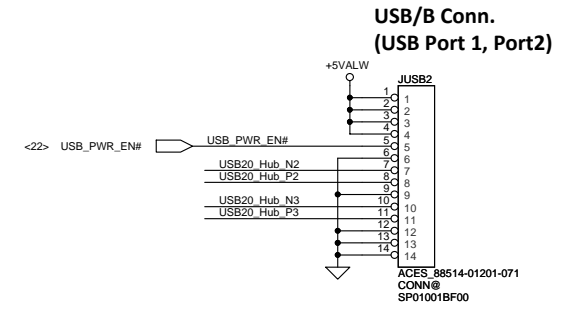
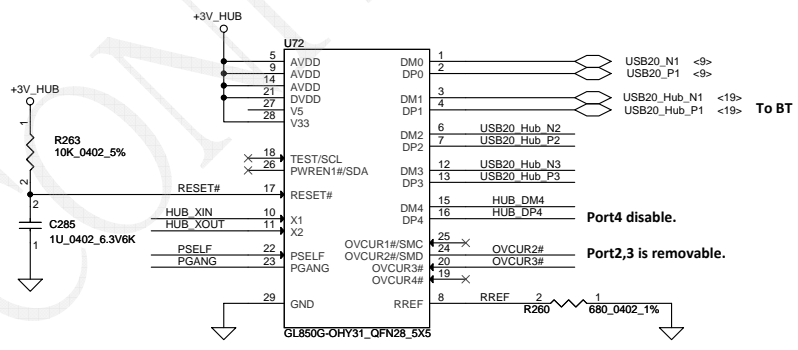
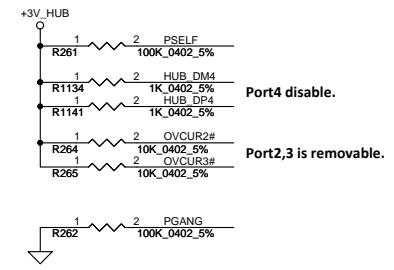
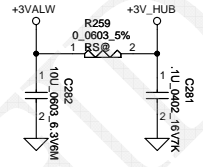
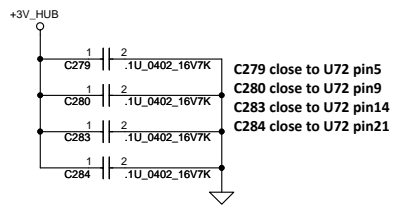
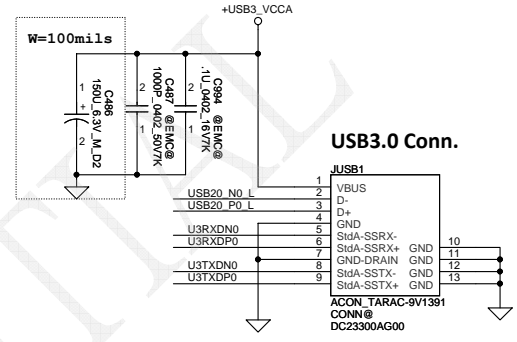
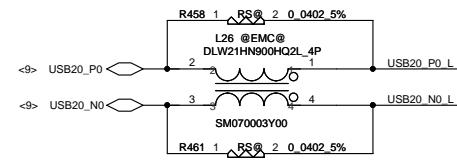
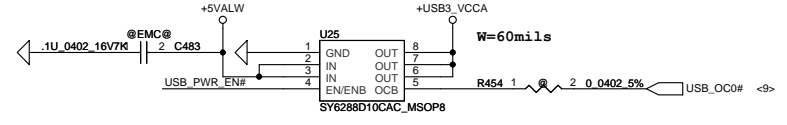
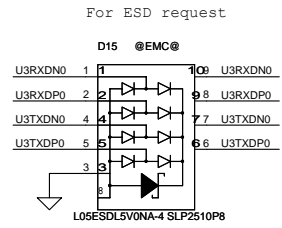
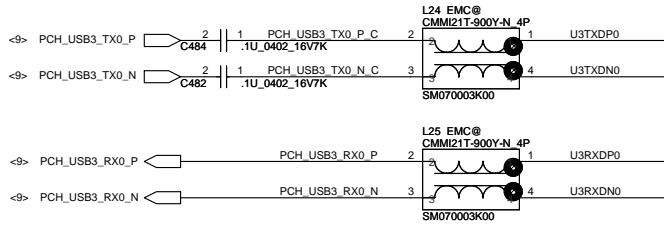
SATA ODD Conn.



FAN1 Conn

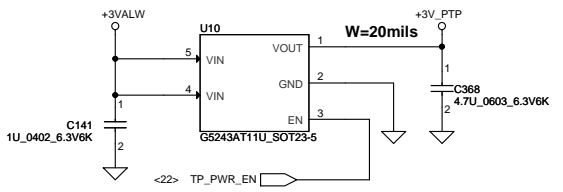
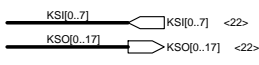
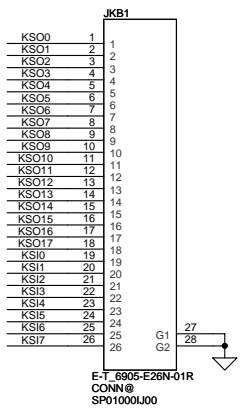


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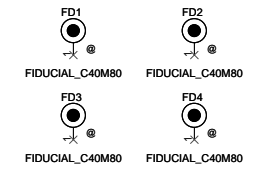
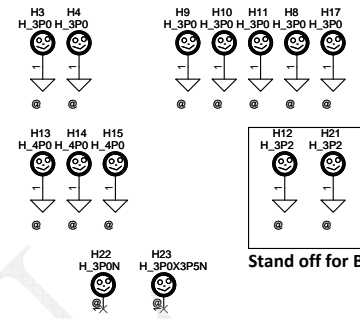
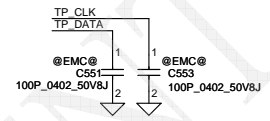
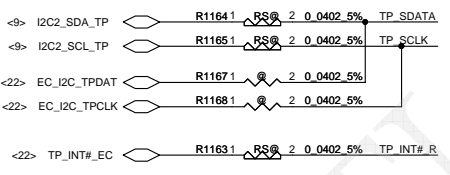
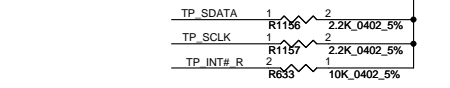
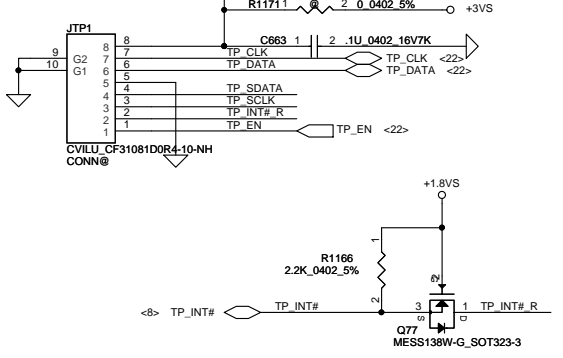


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1.0	Custom Z5WAL Bay Trail M LA-B211P	Monday, April 07, 2014		1.0
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KB Conn.

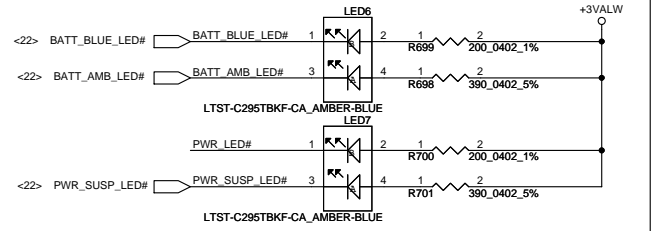


TP module Conn.

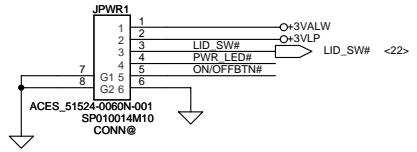


Stand off for BATT/B.

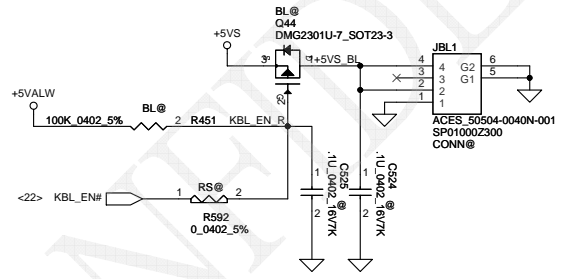
LED



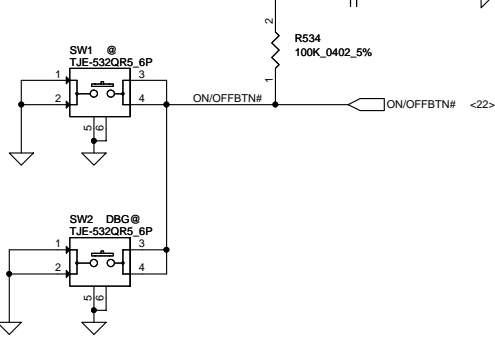
PWR/B Conn.



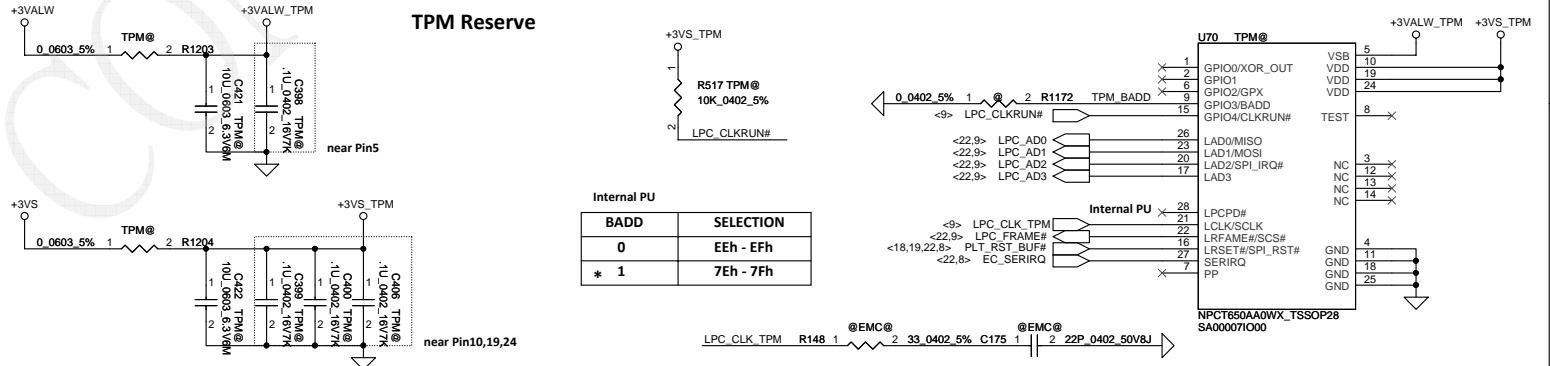
KB BackLight Conn. Reserve



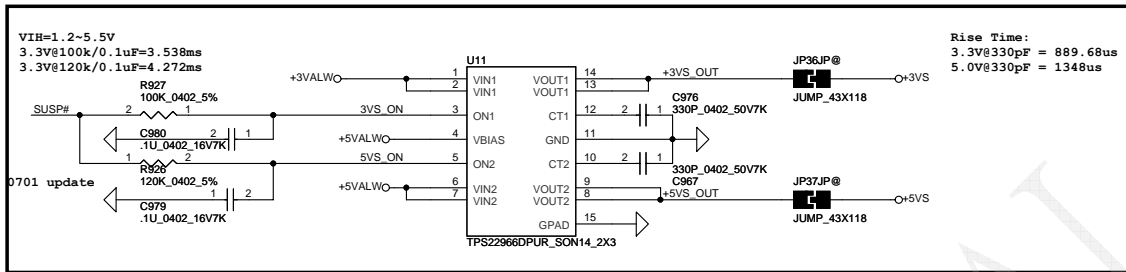
ON/OFF BTN Test only



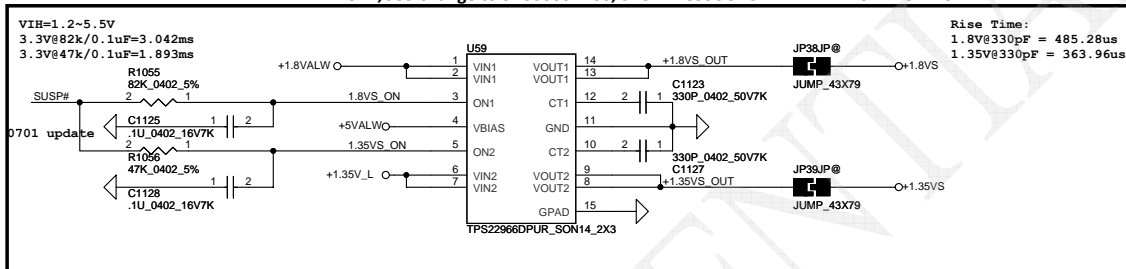
TPM Reserve



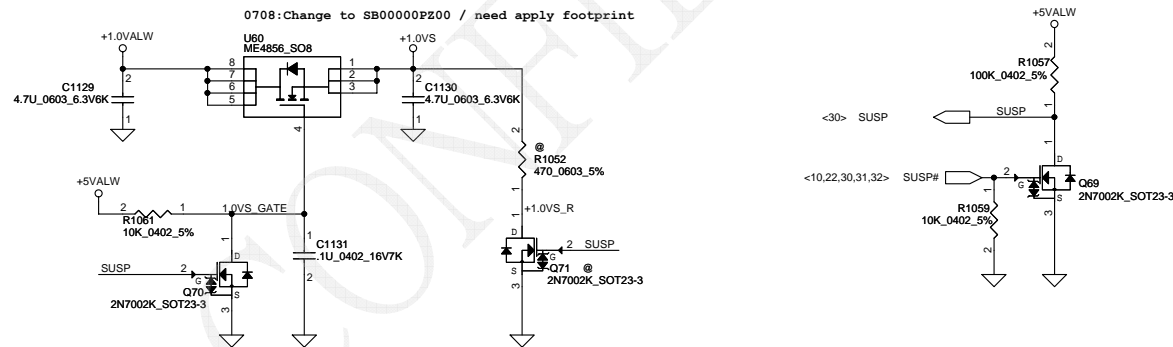
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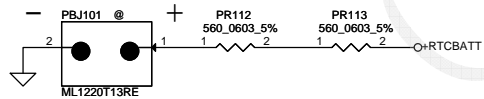
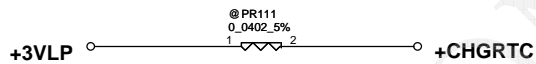
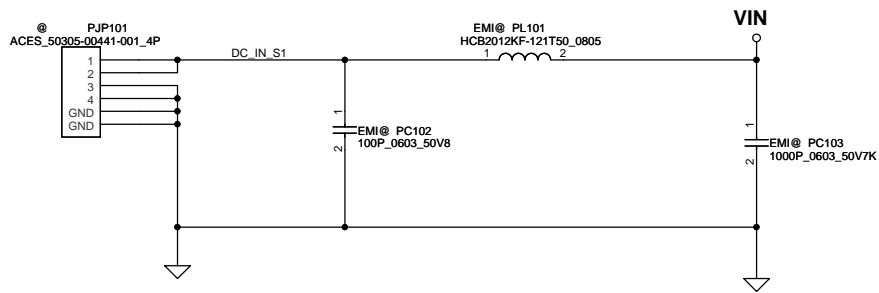
U11,U59 change to SA00006FD00, S IC APE8990GN3B DFN 14P DUAL LOAD SW



+1.0VALW TO +1.0VS



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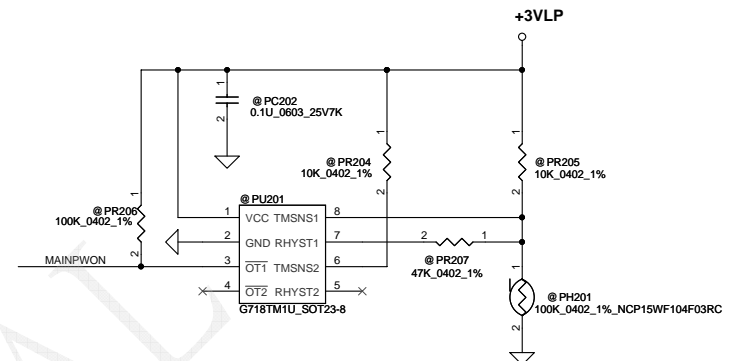
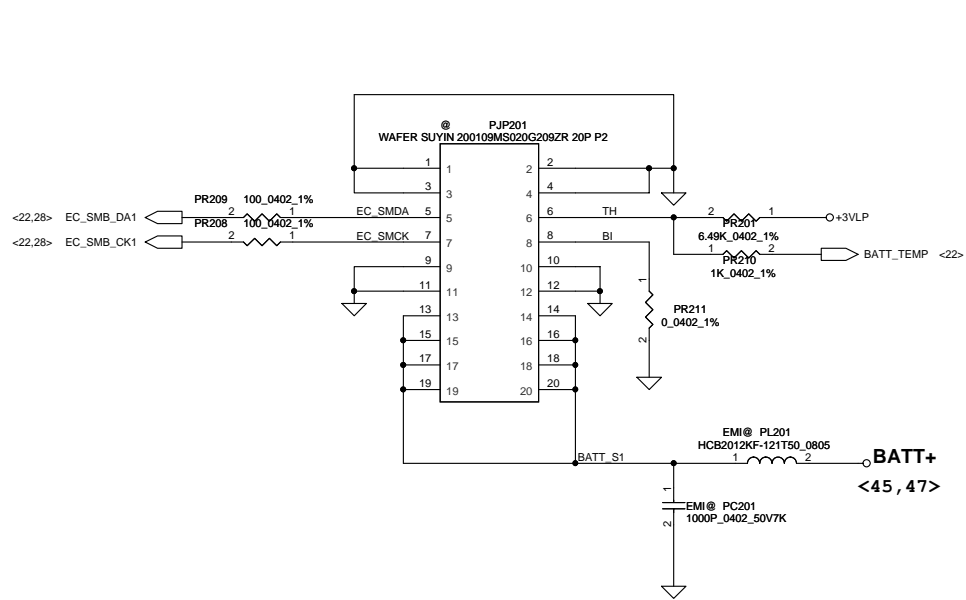
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Compal Electronics, Inc.

DCIN / RTC

Bay Trail M LA-B211P

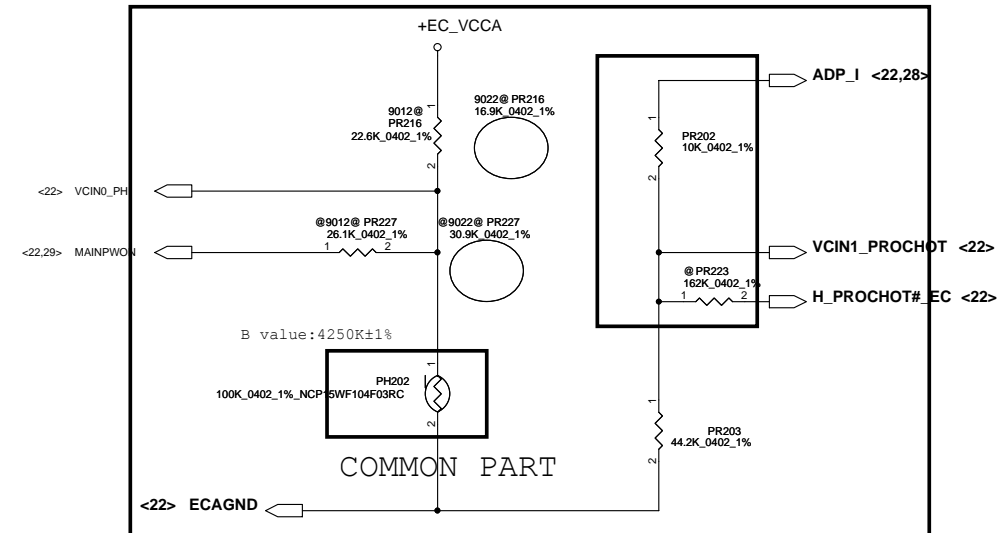
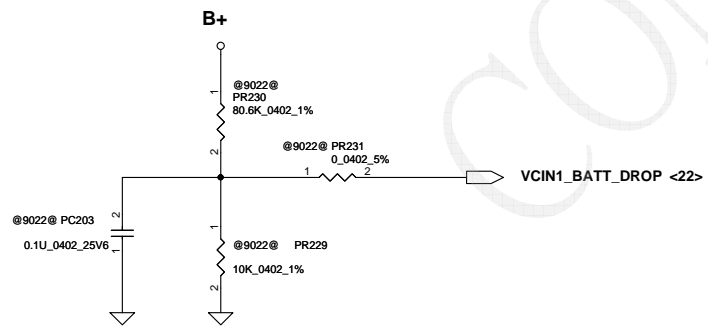
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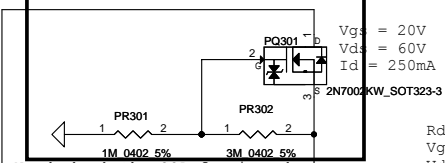
	For KB9012 OTP	For KB9022 OTP
92	1.2V	1.0V
56	1.2V	1.0V
PR216	22.6K ohm	32.4K ohm
PR227	26.1K ohm	30.9K ohm

Need confirm the setting

For KB9012 sense 10mΩ	Active	Recovery
40W	42.8W, 0.43V	34.4W, 0.43V



Protection for reverse input



Rds(on) typ = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)

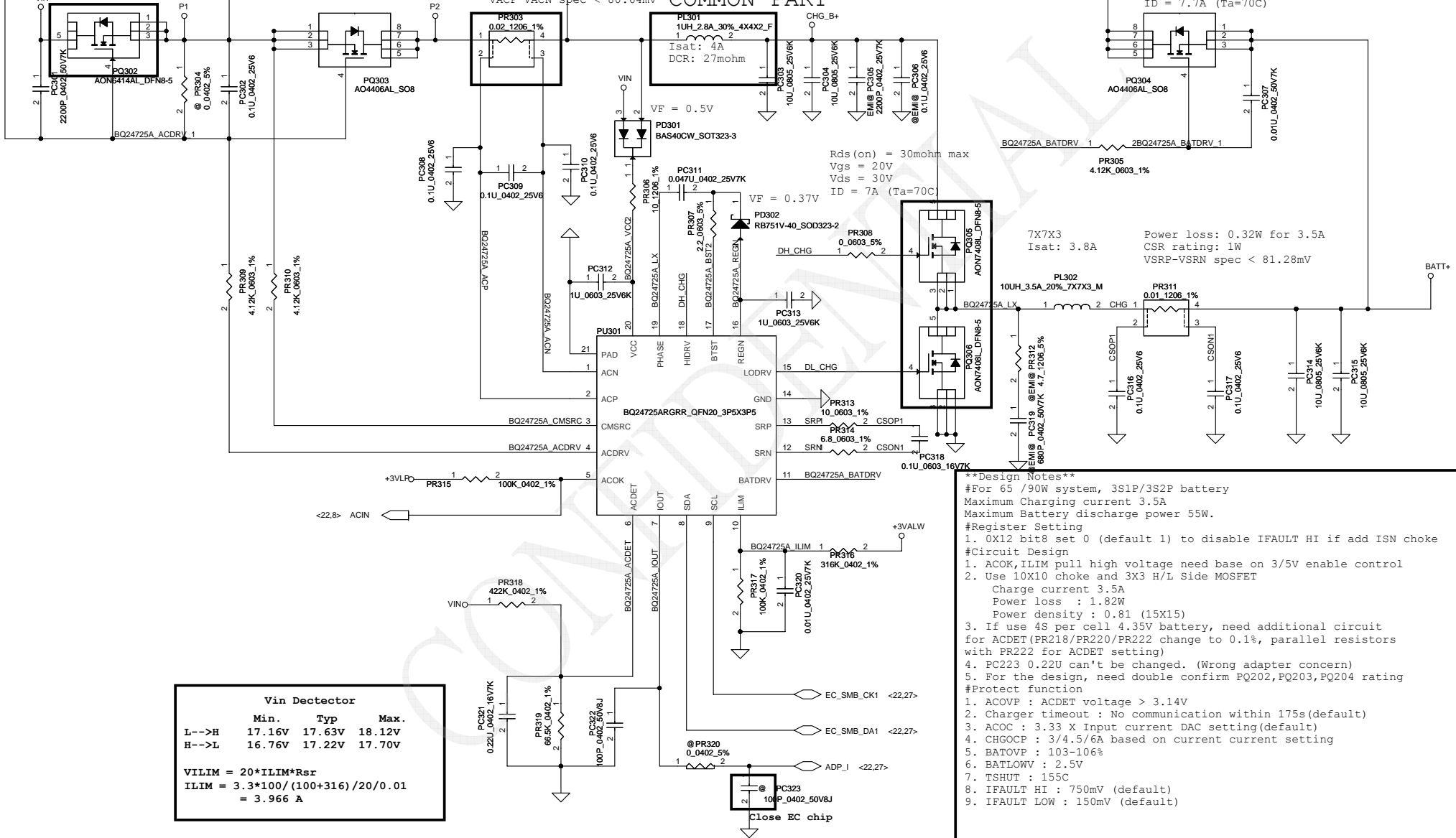
max Power loss 0.22W for 90W; 0.12W for 65W system
CSR rating: 1W
VACP-VACN spec < 80.64mV

COMMON PART

Rds(on) = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)

Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)

Power loss: 0.32W for 3.5A
CSR rating: 1W
VSRP-VSRN spec < 81.28mV



Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rs
ILIM = 3.3*100/(100+316)/20/0.01 = 3.966 A

****Design Notes****

#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W.

#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke

#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L Side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)

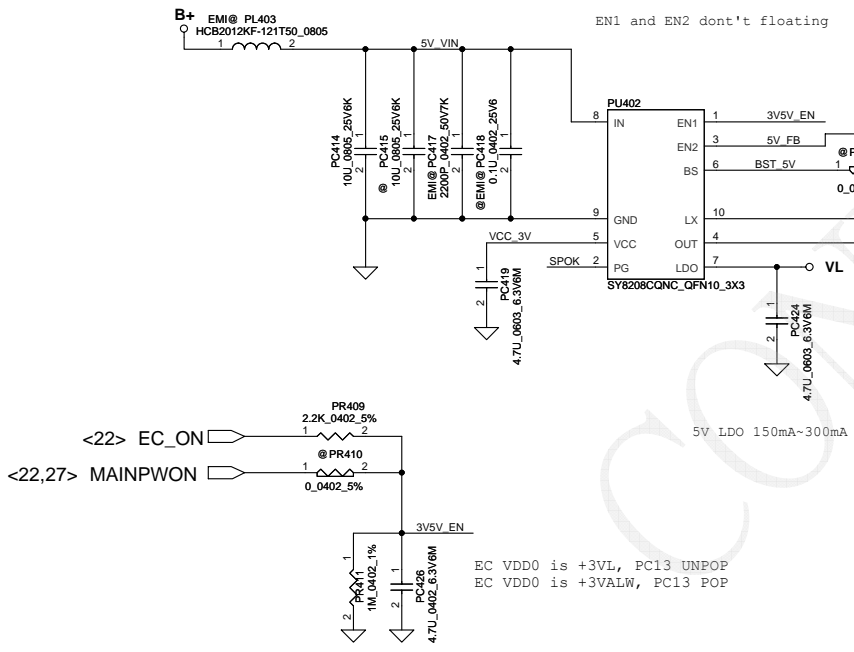
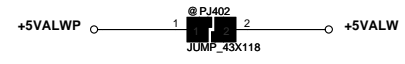
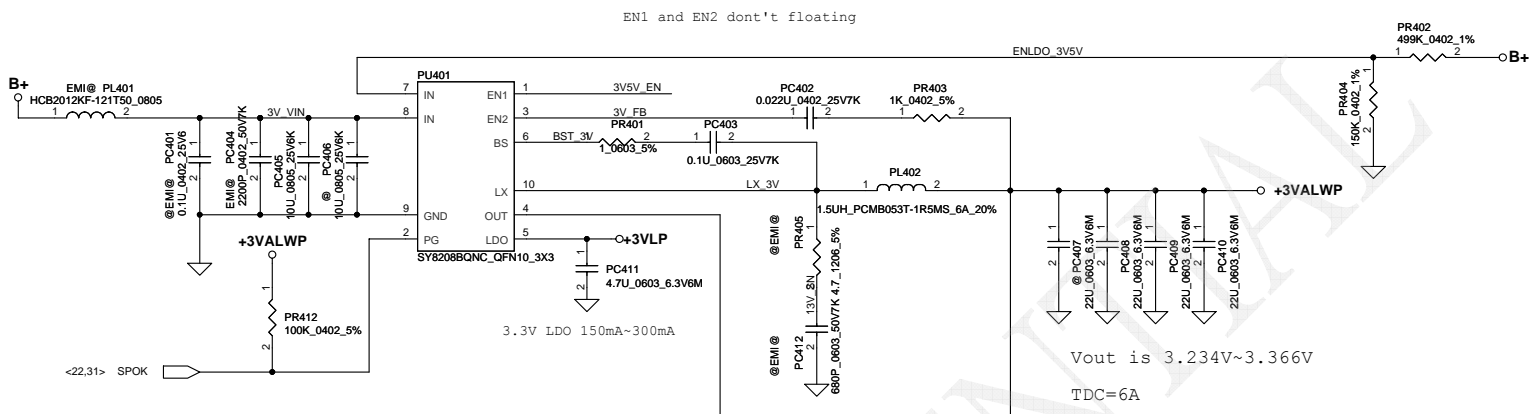
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)

4. PC223 0.22u can't be changed. (Wrong adapter concern)

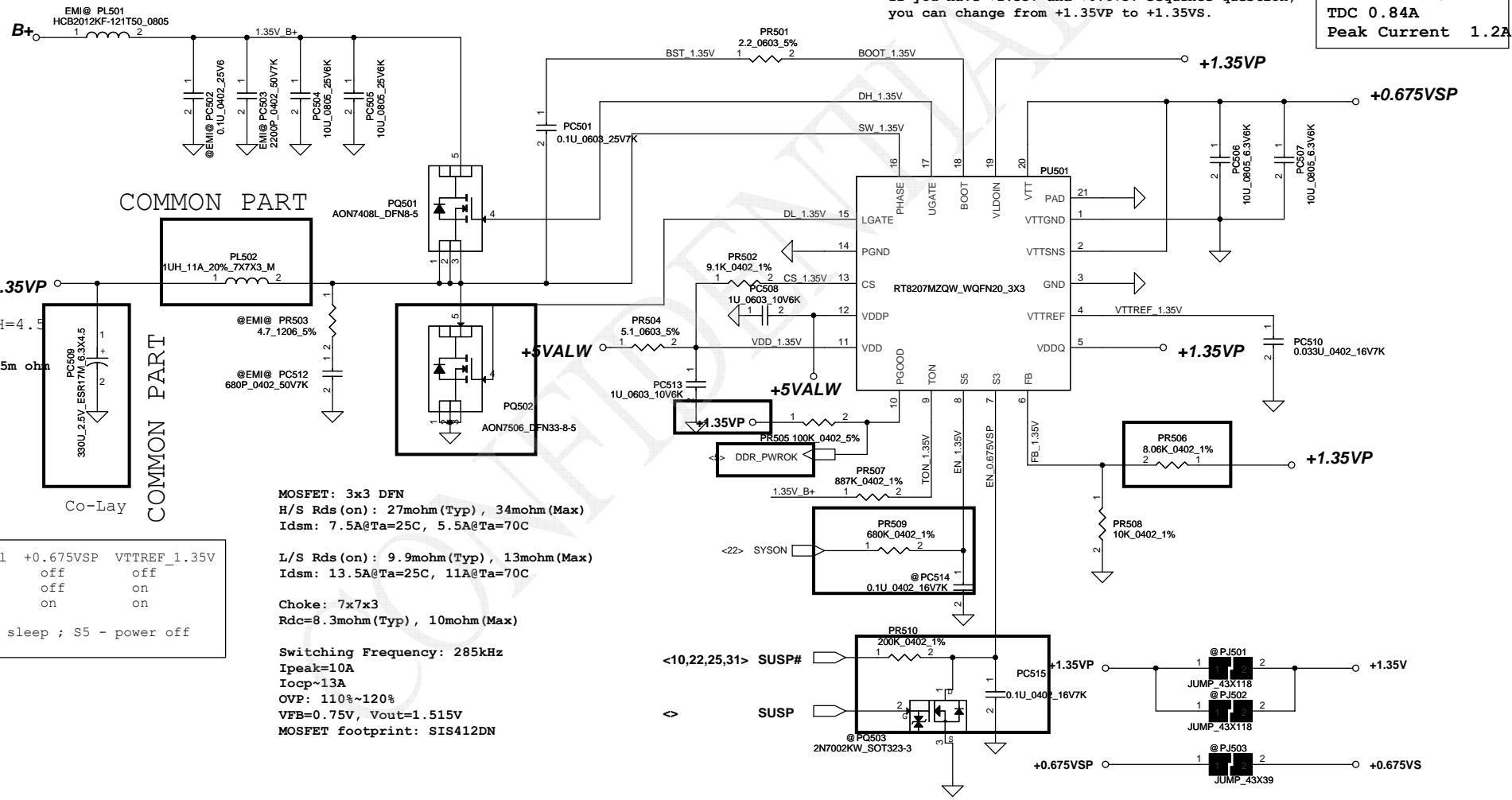
5. For the design, need double confirm PQ202,PQ203,PQ204 rating

#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 150mV (default)

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COMMON PART

COMMON PART

SF000002Z00 H=4.5
ESR=15m ohm

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

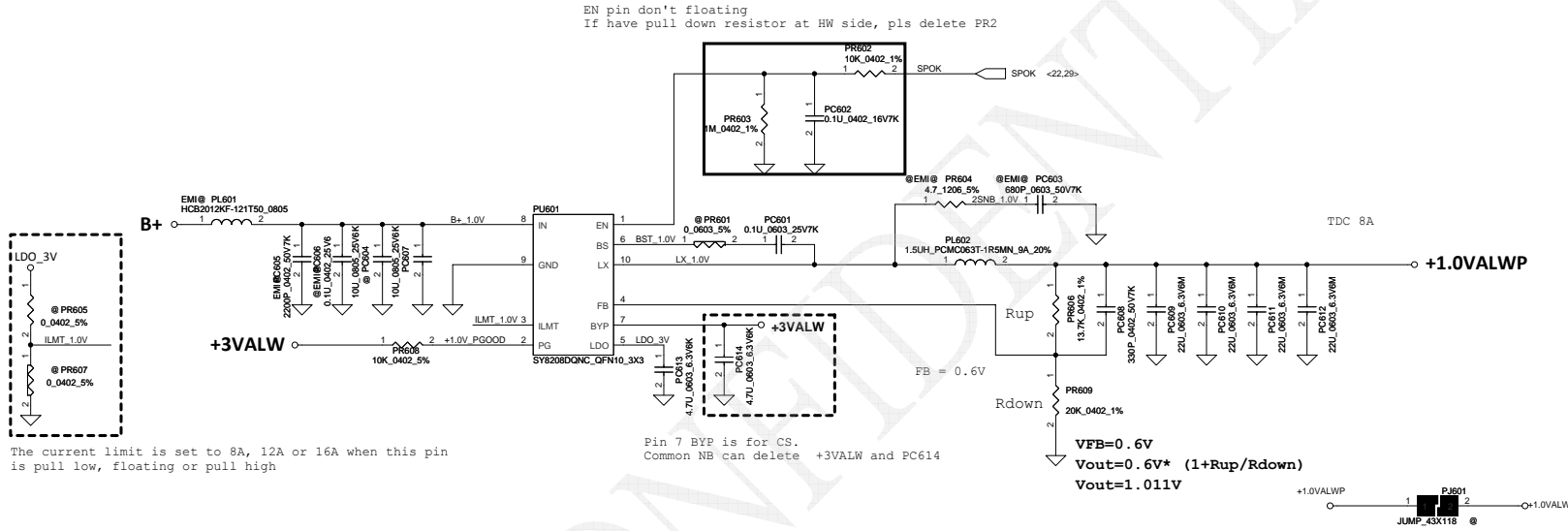
MOSFET: 3x3 DFN
H/S Rds (on): 27mohm (Typ), 34mohm (Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on): 9.9mohm (Typ), 13mohm (Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm (Typ), 10mohm (Max)

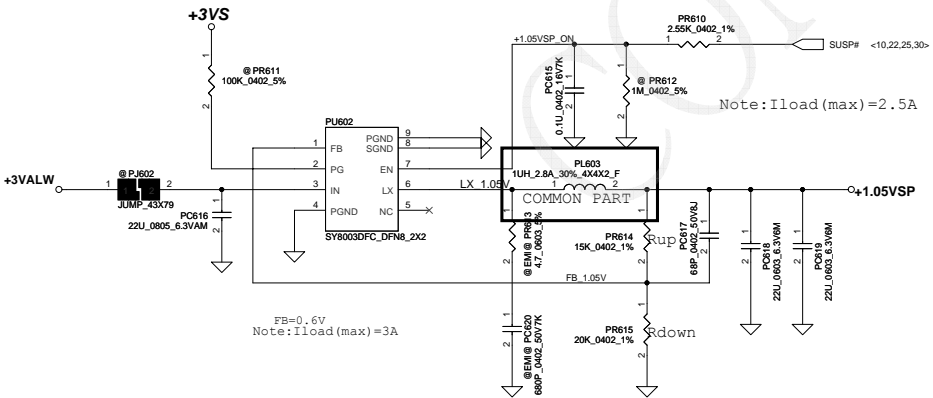
Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFEB=0.75V, Vout=1.515V
MOSFET footprint: SIS412DN

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The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS. Common NB can delete +3VALW and PC614



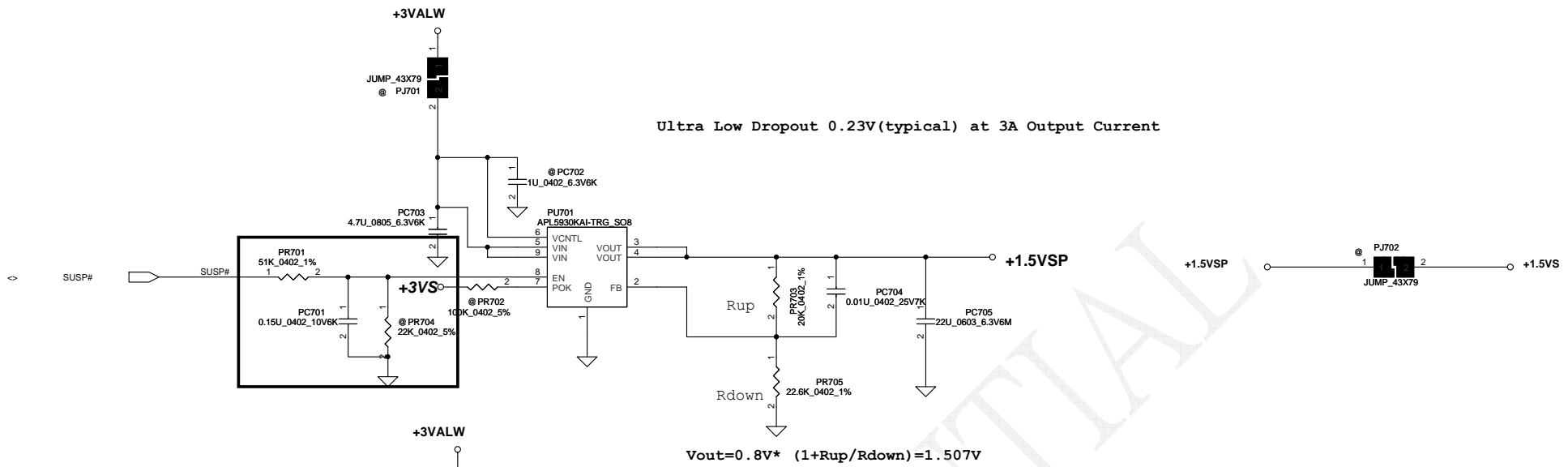
Note: Iload (max) = 3A

Note: Iload (max) = 2.5A

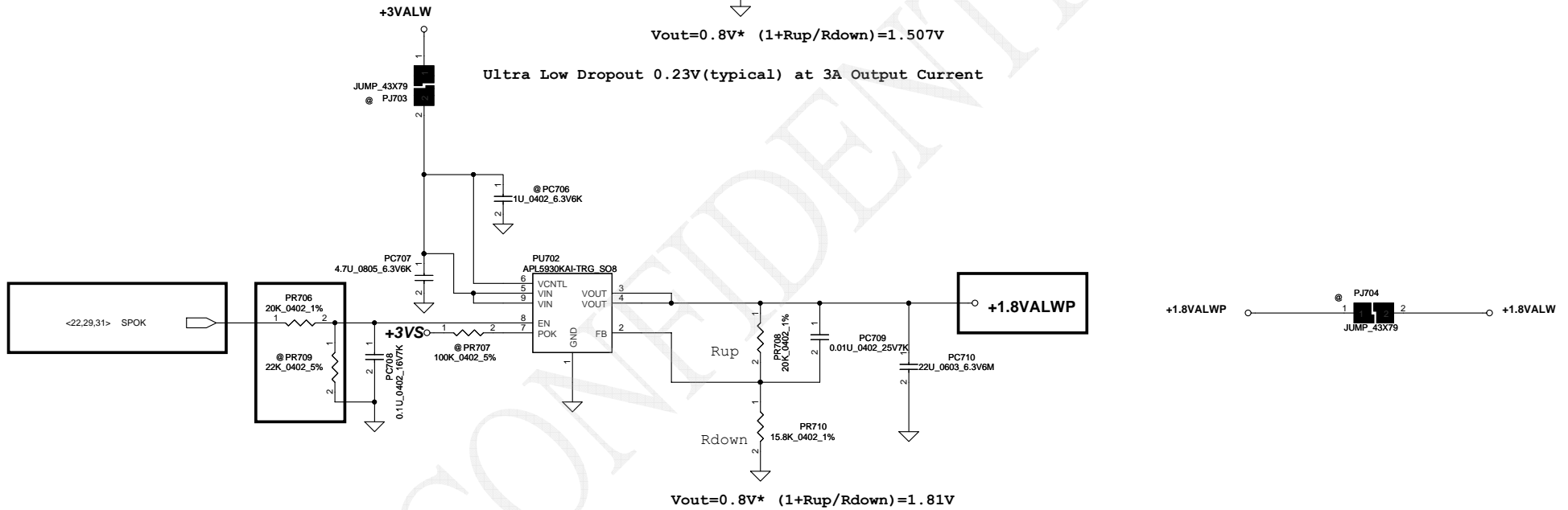


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Ultra Low Dropout 0.23V(typical) at 3A Output Current



Ultra Low Dropout 0.23V(typical) at 3A Output Current



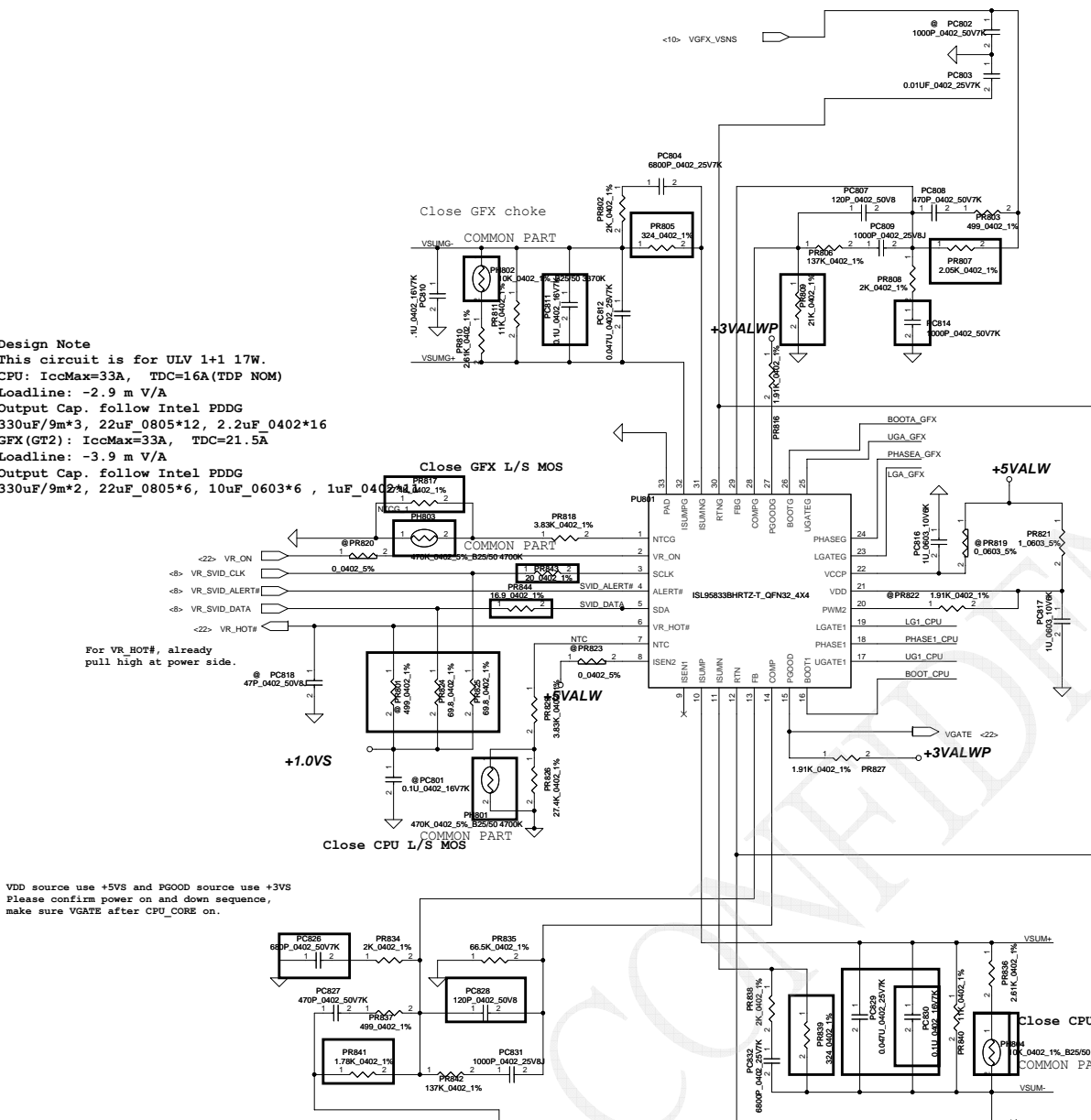
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Design Note
 This circuit is for ULV L1+1 17W.
 CPU: IccMax=33A, TDC=16A(TDP NOM)
 Loadline: -2.9 m V/A
 Output Cap. follow Intel PDDG
 330uF/9m*3, 22uF_0805*12, 2.2uF_0402*16
 GFX(GT2): IccMax=33A, TDC=21.5A
 Loadline: -3.9 m V/A
 Output Cap. follow Intel PDDG
 330uF/9m*2, 22uF_0805*6, 10uF_0603*6, 1uF_0402*4

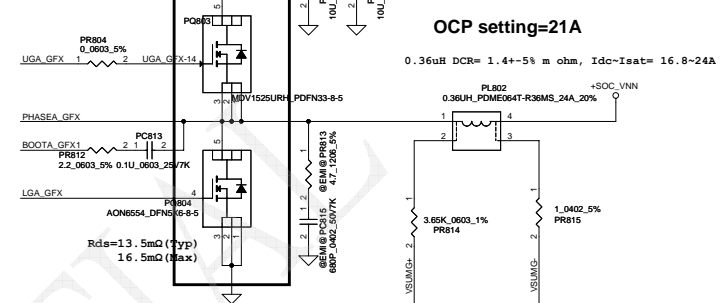
For VR_HOT#, already pull high at power side.

VDD source use +5VS and PG00D source use +3VS
 Please confirm power on and down sequence, make sure VGATE after CPU_CORE on.

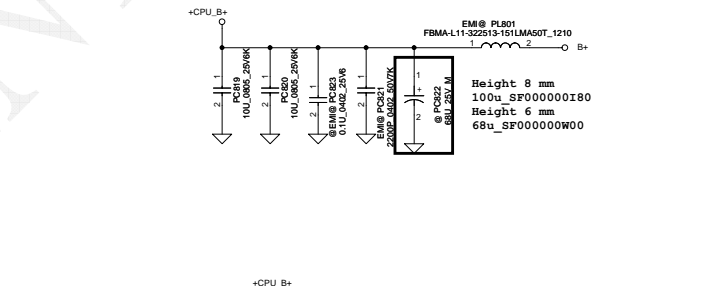
Layout Note
 SVID routing
 1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
 2. SVID spacing requirement is 18mils(0.475mm)
 3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
 4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
 5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.
 6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.



Layout Note
 Reduce Acoustic Noise
 1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
 2. Input ceramic caps must place on symmetry same location on top side and bottom side.



PR817 and PR826
 27.4k ohm for 100 degree
 61.9k ohm for 110 degree



$$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum}) * DCR)$$

If Cn is correctly selected, when the load current has a square change, the output voltage also has a square response.

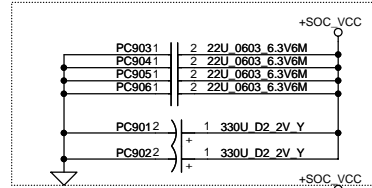
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Issued Date	2013/9/25	Deciphered Date	2014/09/25	CPU CORE/GFX CORE
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PWR Rule
需確認最新SPEC.
Modify 8/6.

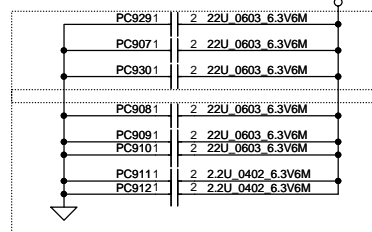
3 X 330u/9m (47W)
 2 X 330u/9m (37W)
 24 pcs 22uF and reserve 4 pcs
 2013/08/16

+SOC_VCC =+CPU_CORE

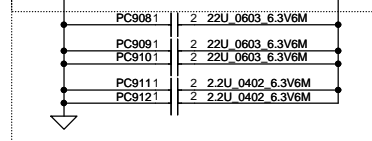
Output Cap
(330uF*2+22uF*4)



Package Edge Cap
(22uF*3)

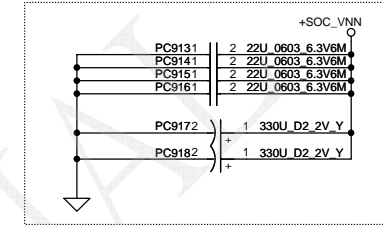


Back Side Cap
(10uF*1+4.7uF*2+2.2uF*2)

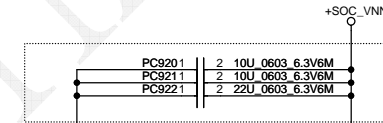


+SOC_VNN =+VGFX_CORE

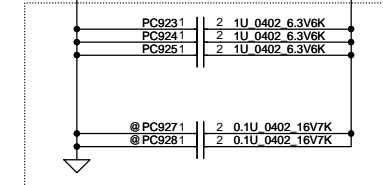
Output Cap
(330uF*3+22uF*4)



Package Edge Cap
(22uF*3)



Back Side Cap
(1uF*3)



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Battery BI pin	for acer server		27	PR211 change to 0_0402_1%	1/10	DVT
2	common part	PH202 change to common part		27	PH202 part number change to SL200002H00	1/10	DVT
3	OTP protect	no hysteresis		27	PR227 change to un-pop	1/10	DVT
4	cost down	chock size change small		28	PL302 change to 10UH_3.5A_20%_7X7X3_M	1/10	DVT
5	MOSFET quality	AO4466L has no good quality		28	PQ303、PQ304 change to AO4406AL	1/10	DVT
6	OTP protect	no hysteresis		29	PC426 change to pop	1/10	DVT
7	rename	for 1.35V lacion		30	@PQ805 change @PQ503	1/10	DVT
8	voltage ripple	change chock value		31	PL602 change to 1.5UH PCMC063T-1R5MN_9A_20%	1/10	DVT
9	CPU tranistion	CPU tranistion test		33	PR839 change to 324_0402_1%		
10					PR814、PR832 change to 3.65K_0603_1%	1/10	DVT
11					PC908、PC909、PC910、PC922		
12					change to 22U_0603_6.3V6M	1/10	DVT
13	OTP protect	no hysteresis		27	PR216 change 16.9K_0402_1%	1/20	DVT
14	ADPI protect	no hysteresis		27	PR202 change to 10K_0402_1%	1/20	DVT
15					PR203 change to 44.2K_0402_1%		
15	no sequence issue	unused part		29	PD401 change to PR410 R-short	2/21	PVT
16	for layout	no placement		34	delt PC919		PVT
17	for layout	no placement		34	delt PC926		PVT
18	for component	BOM change		28	PR308 SD00001FX00 change to SD013000080		PVT
19	common part	PL301 change to common part		28	PL301 change to common part SH00000YG00		Pr-MP
20		Improve part rating		34	Change PC901,PC902,PC917,PC918 from SGA000026800 to SGA20331E10		Pr-MP
21		unused part		29 31	PR407、PR601、PR607change to R-short		Pr-MP
22		symbol change		33	PQ801, PQ803 change symbol name:MDV1525URH_PDFN33-8-5)		Pr-MP
		unused part		33	PC822 change to un-pop		Pr-MP

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Item	Page#	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.15	HW	12/23		Change JCAM1 pin assignment(Follow Z5WAH).	1. Swap JCAM1 pin assignment.	0.3
2	P.17	HW	12/23		Follow VESA CRT connector pin assignment.	1. Connect JCRT1.5 to GND.	0.3
3	P.20	HW	12/23		Connect JHDD1 pin8,9,10 to +3VS.	1. Connect JHDD1 pin8,9,10 to +3VS.	0.3
4	P.19	HW	12/23		Connect JMINI1 pin6,28,48 to +1.5VS_WLAN.	1. Add JP9 for +1.5VS_WLAN. 2. Connect JMINI1 pin6,28,48 to +1.5VS_WLAN.	0.3
5	P.24	HW	12/25		Update codec schematic for vendor and ESD required.	1. Change C1209,C1210 to 4.7uF 0603 size. 2. Reserve R1123 100k,PU +3VS for CPVREF. 3. Change D46 to SCA00001B00. 4. Add L57,L58,C2142,C2143. 5. Change C2141 to SE080105K80.	0.3
6	P.22	HW	12/25		Update EC schematic.	1. Change TXE_DBG to pin99. 2. Add R1169 between EC and SoC for H_PROCHOT#. 3. Reserve Q51,R483 to pin27 for clear CMOS. 4. Change R506 to 15k for DVT board ID. 5. Rename ON/OFF to ON/OFFBTN#.	0.3
7	P.23	HW	12/25		Rename Screw hole(follow Z5WAH).	1. Change H12 and add H21 to H_3P2 for stand-off. 2. Add H8. 3. Del H16,H20.	0.3
8	P.15,19	HW	12/25		Rename Conn.(follow Z5WAH)	1. Rename JRJ45 to JRJ1. 2. Rename JEDP1 to JLVDS1.	0.3
9	P.9	HW	12/25		Correct I2C connection.	1. Change Q80.1 to SOC_I2C5_CLK. 2. Change Q81.1 to SOC_I2C2_CLK.	0.3
10	P.18,22	HW	12/30		Leakage and reserve disable LAN feature.	1. Add R1140 PU to +3V_LAN for LAN_PME# and de-pop R484. 2. Connect U28.106 to U68.38 for disable LAN PHY.	0.3
11	P.23	HW	01/07		Del Screw hole(follow ME drawing)	1. Del H6.	0.3
12	P.25	HW	01/07		SA00004MM00 is X1 code.	1. Change U11,U59 to SA00006FD00.	0.3
13	P.21	HW	01/09		Follow 2014 OSCON standard part.	1. Change C486 to SF000006R00.	0.3
14	P.24	HW	01/09		For codec vendor test result.	1. Change R1109,R1112 to 59ohm,SD000006J80.	0.3
15	P.8	HW	01/09		Rename CLR1 for load BOM error.	1. Rename CLR1 to JCMOS1.	0.3
16	P.24	HW	01/09		Cap. 1uF 0603 change to 0402.	1. Change C2141 to SE000000K80.	0.3

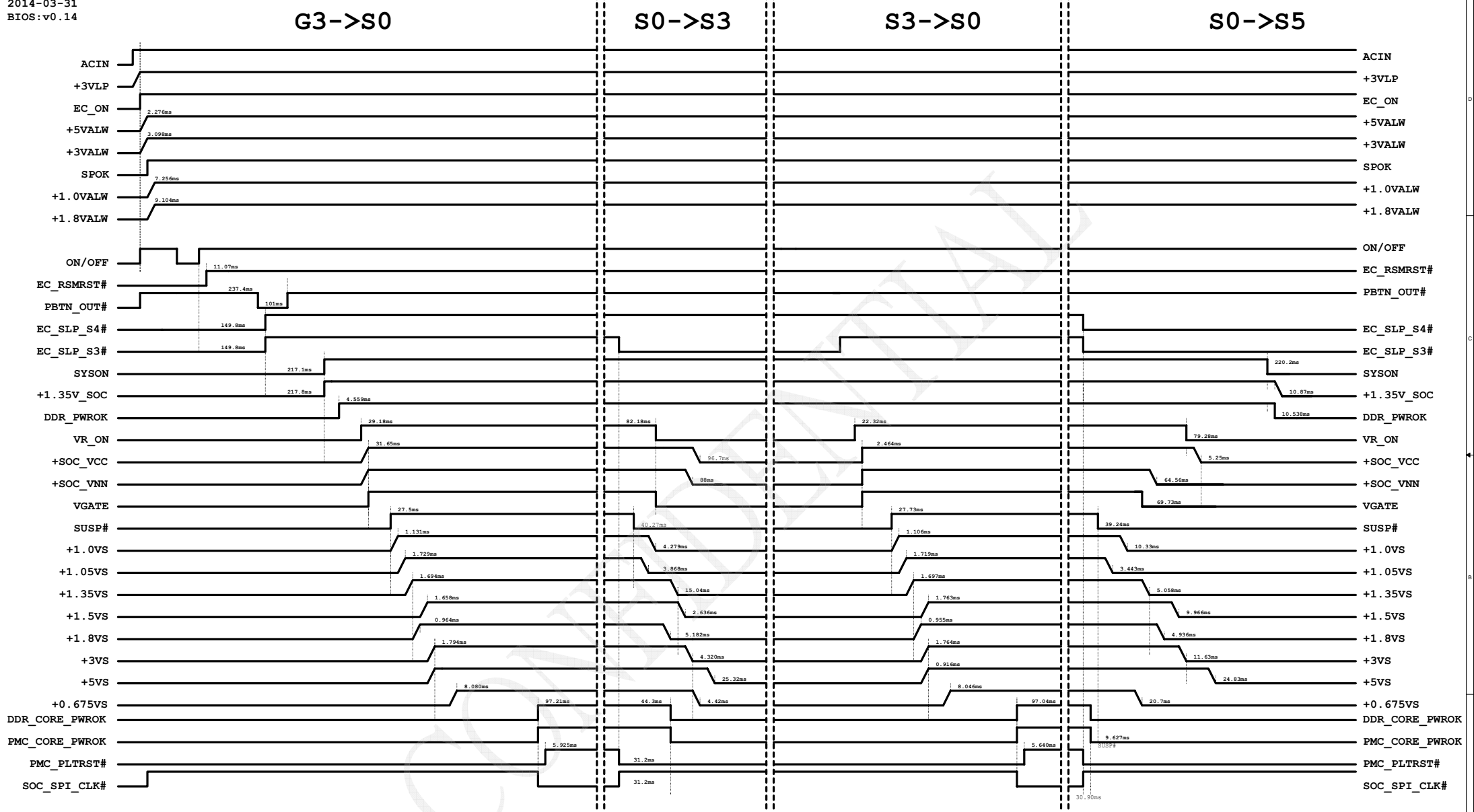
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Item	Page#	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
17	P.21	HW	01/09		Change USB hub solution to GL850G-OHY32.	1. Del U58,R1045,R1046,R1047,R1048,R1049,R1050,C1117,C1118,C1119,C1120,C1121,C1122. 2. Add U72,R259,R260,R261,R262,R263,R264,R265,R1134,R1141,C279,C280,C281,C282,C283,C284,C285,C286,C287.	0.3
18	P.22,23	HW	01/09		TP support wake feature and leakage issue.	1. Add U10,C141,C368,net "TP_PWR_EN" for +3V_PTP and reserve R1170,R1171 for +3VALW,+3VS. 2. Change R478,R479,R633,R1156,R1157 PU to +3V_PTP and pop R1163. 3. Change R1156.1 to TP_SDATA. Change R1157.1 to TP_SCLK.	0.3
19	P.8,9,22,23	HW	01/13		Reserve TPM circuit.	1. Reserve U70,U71,Q83,R148,R496,R517,R1017,R1034,R1172,R1203,R1204,C175,C398,C399,C400,C406,C421,C422. Add R1021,R1025.	0.3
20	P.23	HW	01/14		Change TP conn. type for ME required.	1. Change JTP1 to SP01001AA00.	0.3
21	P.9,21	HW	01/14		Swap USB2.0 port for customer required.	1. Change USB2.0 port0 to USB3.0 connector. Change USB2.0 port1 to USB hub.	0.3
22	P.15	HW	01/14		Separate TS USB/I2C connection(follow Z5WAH).	1. Remove R1146,R1148,R1149,R1151. 2. Change I2C5_SDA_PNL to JLVDS1.21. Change I2C5_SCL_PNL to JLVDS1.22.	0.3
23	P.21	HW	01/14		Height limit issue.	1. Change C486 to SGA00009100,D2 size.	0.3
24	P.8	HW	01/14		Add test point.	1. Add T207 for PMC_SUS_STAT#.	0.3
25	P.23	HW	01/14		For LED brightness(follow Z5WAH's result).	1. Change R699,R700 to 330ohm. Change R698,R701 to 560ohm.	0.3
26	P.8,15,18	HW	01/16		Unused part.	1. Change R998,R1124,R1162 to R-short.	0.3
27	P.8,18	HW	01/16		For crystal vendor test result.	1. Change C1009,C1010 to 18pF. 2. Change C1236,C1237 to 15pF and add R1202.	0.3
28	P.15	HW	02/21		Reserve +3VS for touch screen.	1. Reserve R1146. 2. Rename net +5V_TS to +TS_PWR.	0.4
29	P.25	HW	02/21		Fine tune sequence.	1. Pop C1131.	0.4
30	P.22	HW	02/25		For PVT board ID.	1. Change R506 to 20k ohm.	0.4
31	P.5	HW	02/25		Add new SoC.	1. Add N2830,N2930,N3530.	0.4
32	P.8	HW	02/27		Cover pad for unused part.	1. Change U54 footprint to TXB0108PWR_TSSOP20-S.	0.4
33	P.23	HW	03/03		Change TP connector symbol.	1. Change JTP1 to CVILU_CF31081D0R4-10-NH_8P-T.	0.4

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34	P.23	HW	03/03		For LED brightness(follow Z5WAH's result).	1. Change R699,R700 to SD034200080,200ohm. Change R698,R701 to SD028390080,390ohm.	0.4
35	P.24	HW	03/03		For audio "Bo" noise issue.	1. Change R1109,R1112 to SD013000080,0ohm. Change R1110,R1113 to SD014604A80,60.4ohm.	0.4
36	P.6,8, 11,15, 16,20, 21,22, 23,24	HW	03/03		Unused part.	1. Change R368,R369,R370,R371,R372,R373,R374, R375,R427,R428,R458,R461,R1022,R1023,R1033, R1088,R1164,R1165,R1169,R1142 to R-short,0402 size. 2. Change R259,R1092,R1093,R1098,R1099,R1201 to R-short,0603 size. 3. Change R1154,R1155 to R-short,0805 size.	0.4
37	P.13	HW	03/03		For ESD reserved.	1. Reserve C166,C167.	0.4
38	P.23	HW	03/05		Debug part.	1. Depop SW1,SW2.	0.4
39	P.5,23	HW	03/06		For ESD.	1. Add C408,0.1uF. 2. Change C1159 to SE070473Z80,0.047uF.	0.5
40	P.10,13, 14	HW	03/06		For EMI.	1. Remove JP4. Reserve L61,L62,L63. 2. Add JP5 and net +1.35V_L. Reserve L59,L60.	0.5
41	P.8	HW	03/06		SLP_S3# leak voltage(follow Z5W1M).	1. Change Q83 direction.	0.5
42	P.8	HW	03/21		Change material to common part.	1. Change C1159 to SE00000MJ00. 2. Change C1003,C1004 to SE071100J80.	1.0
43	P.15	HW	03/21		For +INVPWR_B+ short protect.	1. Pop R959.	1.0
44	P.22	HW	03/21		For Pre-MP borad ID.	1. Change R506 to 27k ohm.	1.0
45	P.22	HW	03/25		For PMC_CORE_PWROK falling time.	1. Change C1157 to R485, 100k ohm.	1.0
46	P.8,22, 23	HW	03/25		Unused part.	1. Change R1015,R1163 to R-short,0402 size. 2. Change R1094,R1095,R1096,R1097 to R-short, 0603 size. 3. Change R236,R237 to R-short,0805 size.	1.0
47	P.18	HW	03/25		Reserve LAN power.	1. Del J8 and reserve R238.	1.0
48	P.5	HW	04/07		Update CPU PN.	1. Update CPU PN to MP version.	1.0

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